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ZTO Thin film transistor parameter extraction and modeling

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"You are never given a wish without also being given the power to make it true. You may have to work for it, however."
Richard Bach

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Abstract

Transistor models are of utmost importance for device behaviour prediction and circuit design. Physical modelling has the advantage of the parameters being correlated based on device physics. This allows to gain insight on the device during the analysis and extraction of parameters phase. However, the extraction methods may not consider possible non-idealities of the device, which can cause modelling issues when working with novel thin film transistors (TFTs).

A simple physical DC and AC model was applied to a novel zinc tin oxide TFT annealed at low temperatures (200 ºC). The characteristic curves of four devices with different dimensions were measured and analysed, and the model parameters were extracted. The characterization and optimization of the models were implemented through the analysis of the fitting with the measured data. Two DC models were developed, the main difference being the contact resistance extraction - using the classic transmission-line method or a procedure based on MOSFETs with non-ideal behaviour that considers the possible bias dependency of the parameter. The latter method allowed to simulate the device characteristic curves more effectively. The AC model did not fit for frequencies above the cut-off and differed slightly for lower frequencies due to the simplicity of the model applied.

Keywords: Semiconductor device modeling, Thin film transistors,Parameter extraction, Contact resistance

Resumo

Os modelos de transístor são de extrema importância para a previsão do comportamento dos dispositivos e design de circuitos. Os modelos físicos possuem a vantagem de existir uma correlação entre os parâmetros extraídos e a física por detrás do dispositivo. É possível assim obter informações sobre o transístor durante a fase inicial de extração de parâmetros. No entanto, os métodos de extração podem não considerar possíveis não-idealidades do dispositivo, o que pode levar a erros durante a criação do modelo para novos transístores.

Um modelo físico DC e um modelo físico AC foram aplicados a transístor de filme fino de ZTO recozido a baixas temperaturas (200 ºC). As curvas características de quatro dispositivos com diferentes dimensões foram medidas e analisadas, e os parâmetros do modelo DC foram extraídos. A caracterização e otimização dos modelos foram implementadas através da análise da comparação com os dados medidos. Foram desenvolvidos dois modelos DC, sendo a principal diferença o método de extração de resistência de contato - usando o método de linha de transmissão clássico ou um procedimento baseado em MOSFETs com comportamento não ideal, que considera a possível dependência do parâmetro em valores de tensão aplicados. O último método permitiu simular as curvas características do dispositivo de forma mais eficaz. O modelo AC não se adequava às frequências acima do corte e diferiu ligeiramente para frequências mais baixas devido à simplicidade do modelo aplicado.

Palavras-chave: Modelização de dispositivos semicondutores, Transístor de filme fino, Extração de parâmetros, Resistência de contacto

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List of symbols

κ	Dielectric constant.
α	Power parameter.
λ	Channel length modulation parameter.
ΔL	Channel length modulation parameter.
μ_{eff}	Transistor channel mobility.
A_i	Transistor current gain.
C_i	Gate dielectric capacitance per area.
Cch	Gate/channel Capacitance.
Covd	Drain overlap capacitance.
Covs	Source overlap capacitance.
f_T	Frequency at which the modulus of the short circuit current gain is unity.
gm	Transconductance.
I_{DS}	Drain-source current.
K	Transconductance parameter.
L	Transistor channel length.
poly-Si	Poly-Silicon.
R_D	Parasitic resistance on the drain contact of the transistor.
R_{DS}	Parasitic resistance on the source and drain contacts of the transistor.
R_S	Parasitic resistance on the source contact of the transistor.
S Parameters	Scattering parameters; a type of high frequency parameters used to describe circuits in terms of wave propagation.
V_{DS}	Drain-source voltage.
V_{GS}	Gate-source voltage.
V_T	Threshold voltage.
V_A	Early Voltage.

W	Transistor channel width.
z_0	Characteristic impedance of a line.

Acronyms

AC	Alternating Current.
DC	Direct Current.
IGZO	Indium Gallium Zinc Oxide.
MOSFET	Metal Oxide Field Effect Transistor.
TFT	Thin Film Transistor.
ZTO	Zinc Tin Oxide.

Objective

This project was realized at the University of Cambridge, in collaboration with CENIMAT in the scope of the BET-EU european project (grant agreement 692373). The main aim of this project is to analyse and apply a physical model to a zinc tin oxide thin film transistor. Transistor models are of utmost importance as they allow us to predict the behaviour of a device, and are necessary to the design of complex circuits. By studying the parameters and the fitting of a physical model to the device we can gain insight to physical phenomena happening within a transistor. The proposed objectives for the thesis are the following:

1. Perform electrical measurements on the fabricated TFTs, regarding capacitance-voltage, transfer and output-voltage characteristics;
2. Obtain a full set of device parameters needed for the compact TFT modeling, using the aforementioned measurements;
3. Apply the parameters to the physical models (both large-signal and small-signal);
4. Optimize the model fitting on the transistor's characteristic curves and analyse the fitted parameters.

1 Introduction

1.1 Thin film transistor

The thin film transistor (TFT) is a field effect transistor that operates on the same basic principles as the metal oxide field effect transistor (MOSFET). It is a device with three terminals (gate, source and drain) made by depositing thin films in a wafer independent substrate. Regarding its structure, the main difference between the TFT and the MOSFET relies on the substrate; the former uses mainly non-conducting substrates such as glass, and the latter uses semiconductor substrates such as a silicon wafer. The use of glass as a substrate presents advantages such as transparency and low transmission of liquid and vapor water [1] (which prevents damage to the device) making TFTs very useful for their application in display technology. Presently, the use of flexible displays is shifting the attention from glass to polymeric substrates, and new applications of TFTs in wearable devices, sensors and biomedical systems are being developed[2, 3, 4].

1.1.1 Device structure and behaviour

The basic TFT consists of a semiconductor active layer, a dielectric and three electrodes named source, drain and gate. Various structures can be arranged (Figure 1.1) depending on the position of the source and drain contacts relative to the gate (top or bottom gate) and the semiconductor layer (staggered when separated by the semiconductor layer, coplanar when on the same side).[5]

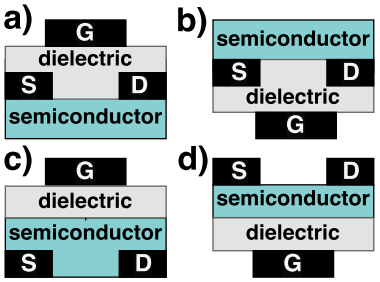


Figure 1.1: TFT architectures a)Top gate; staggered b)Bottom gate; staggered c)Top gate; coplanar d)Bottom gate; coplanar

The TFT operates identically to the MOSFET in the manner that a tension applied to the gate will turn the device on or off, controlling the current flow between the source and drain electrodes. Depending on the threshold voltage (V_T) needed for the device to function, a TFT can be defined as an enhancement-mode device (for N-type if $V_T>0$) or as an depletion-mode device (for N-type if $V_T<0$). Ideally it will act like a capacitor where the charges accumulate at the interface between the semiconductor and dielectric when a certain gate bias is applied.

The differences start in the operation zone, as the TFT operates in the accumulation condition while a MOSFET operates normally in the inversion. The operation zone is reflected in the current flow as the conduction channel is created by the accumulation of majority carriers. This means that there is no inversion in the polarity of induced carriers, which creates difficulty in defining the accumulation threshold.[6] The disorder of the semiconductor channel layer also creates difficulty in perceiving the V_T, due to the existence of localized deep and shallow traps in the band-gap. The density of carriers trapped in those states can be superior to the density of free carriers, which means that the trap states determine the behaviour of field-effect mobility as a function of gate bias.[6]The absence of a depletion region is another distinction from the MOSFET, as the TFT device is not isolated from the substrate nor has a p-n junction near the contact preventing the current flow before the channel formation.

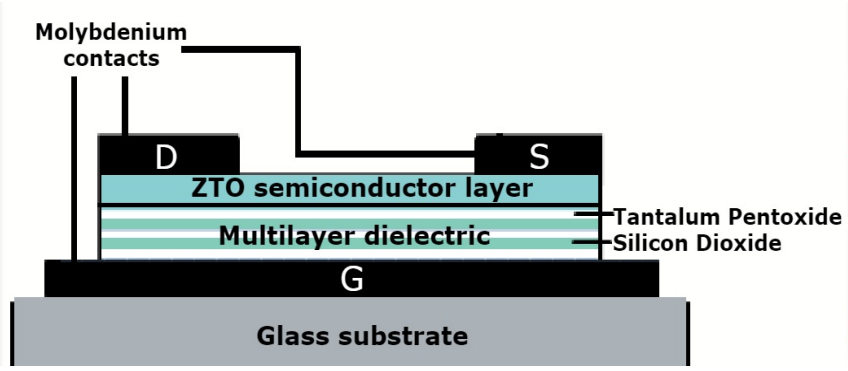


Figure 1.2: Zinc tin oxide TFT structure and materials

1.1.2 Materials and production techniques

TFTs with an amourphous silicon active layer are the most commonly fabricated in large scale electronics due to its low cost. However other types of materials as the higher mobility polycristalline silicon(poly-Si), metallic oxides and organic semiconductors are also used when fabricating TFTs. There is a strong interest in oxide TFTs as they have shown to possess high transparency, good environmental stability, reproducibility and can exhibit mobilities comparable to poly-Si.[7, 8, 9] . That interest started predominantly for Indium Gallium Zinc Oxide (IGZO), and since 2012 has been observed the commercialization of products containing this material.Yet, due to the scarcity of gallium and indium, the costs related to this oxide are subject to increases. This stimulated the search for a substitute. Amongst the different oxide materials investigated, Zinc Tin Oxide (ZTO) has shown to be a possible alternative to IGZO, as tin is an abundant and inexpensive metal that has a similar electronic configuration to indium. The low cost and high transparency of ZTO (due to the high optical band gap) and the possibility of an environmentally friendly deposition process make it an attractive replacement. [7]

The materials used in the thin film transistor dielectric are normally insulating materials with high values of dielectric constant (high-κ) in order to obtain a higher gate capacitance with miniaturization.[10] The issue with high-κ materials is that they may exhibit a low bandgap energy which can allow for electrons to tunnel across the dielectric. This can be solved with the use of a multilayer dielectric, for example, that combines the high-κ material with silicon oxide, limiting the leakage and still obtaining a good capacitance value.[11]

The device used in this project is a vacuum-processed NMOS ZTO TFT with a multilayer TaO_5/SiO_2 dielectric in a corning glass substrate (Figure 1.2) annealed at 200 °C. A higher annealing temperature would have a reduction effect on the deep and shallow states due to the decrease of intrinsic defects such as oxygen vacancies, thereby making the device more stable.[12] However, a lower temperature of annealing is preferred as it allows for a lower cost of fabrication and possible use on flexible electronic applications. Nevertheless, the non-ideal behaviour of the device creates a significant need for models capable of interpreting its performance.

1.2 Device Modeling

Device modeling plays a crucial role in today's method of representing and analysing the operation of electronic devices. Compact models able to be applied in circuit simulating software are needed in order to simulate and predict the behaviour of devices in circuits or more complex systems. As the complexity of solid state devices increases, the search for simple models that can provide a good approximation to the device operation while taking into account the various special physical phenomena and non-linear behaviour becomes more necessary. We can consider three different categories of semiconductor device models:

- Physical - Provides physical insight to the performance properties, allowing to predict the behaviour even when exists parameter variation. But it may fail for devices where there is lack of information about the phenomena governing processes;[13]
- Empirical - Computational model that can often give reasonable results for devices with no prior experimental data. However is only based on fitted data, being difficult to extrapolate to other devices or dimensions;
- Semi-Empirical - Calculated with adjustable parameters fitted to experiments or first-principles calculations.[13]

In the following parts of the project the physical model will be the adopted model type.

1.2.1 DC Model

A DC Model is a numerical relation that relates the terminal voltages to the currents of the device at dc and low frequencies.[14]In the case of N-type MOSFET devices, we can write the drain-source current (I_{DS}) as a function of the voltages between the gate and source (V_{GS}) and the source and drain (V_{DS}) using the equations[15]:

$$I_{DS} = \begin{cases} \text{Subthreshold Current} & V_{GS} < V_T \text{ Subthreshold region} \quad (1.1a) \\ \mu_{\text{eff}} C_i \frac{W}{L}[(V_{GS} - V_T)V_{DS} - V_{DS}^2] & V_{DS} < V_{GS} > V_T \text{ Linear region} \quad (1.1b) \\ \frac{1}{2}\mu_{\text{eff}} C_i \frac{W}{L}[V_{GS} - V_T]^2 & V_{DS} > V_{GS} > V_T \text{ Saturation region} \quad (1.1c) \end{cases}$$

Where W represents the channel width, L the channel length, μ_{eff} the channel mobility, C_i the gate dielectric capacitance per area, V_T the threshold voltage. $\mu_{\text{eff}}C_i$ can also be represented by the transconductance parameter (K).

On TFTs we can observe the presence of a various effects, due to special physical phenomena or bias and geometry dependence of parameters, that are not included in the ideal transistor model and that should be described.

1.2.1.1 TFT model

One of the differences that make the MOSFET model unable to interpret the TFT behaviour is the effect of the often nonlinear series resistance (R_{DS}). This parasitic resistance is mainly due to the regions connecting the metal contacts of the source and drain to the transistor channel.[16] The influence is especially observed in small channel devices, where the device's transconductance does not increase as expected when the channel length (and therefore the

channel resistance) is reduced. The voltage on the internal terminals of the TFT is significantly less than the voltage applied to the drain and source contacts . This is due to the voltage drop on the contact resistance. [17] We can observe in Figure 1.3 the TFT structure of the model including the intrinsic TFT and contact resistances.

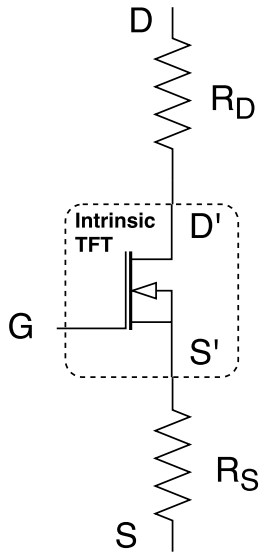


Figure 1.3: TFT structure with contact resistance

The voltages $V'_D$and V'_S control the current in the channel, and relate to it and the contact resistance by the equations [18]:

$$V'_{GS} = V_{GS} - I_{DS}.R_S = V_{GS} - I_{DS}\frac{R_{DS}}{2} \tag{1.2}$$

$$V'_{DS} = V_{DS} - I_{DS}(R_S + R_D) = V_{DS} - I_{DS}R_{DS} \tag{1.3}$$

Being that the previous equations are only correct if we assume the symmetry of the device (in other words R_{DS}=R_D+R_S).

According to the model of Servati et al.(2003), we can represent the above threshold behaviour of a TFT considering the contact resistance, the I_{DS} carrier velocity saturation that has a dependence on the V_{GS} voltage [15] and other non-ideal effects. The power parameter (α) relates to the carrier velocity saturation effect, which could lead to inaccuracies if it was assumed to be two like in MOSFET devices. The model is described by the following equations [18]:

$$I_{DS} = \begin{cases} K\frac{W}{L_{eff}}(V_{GS} - V_T - \frac{V_{DS}}{2})^{\alpha-1}(V_{DS} - I_{DS}R_{DS}) & \text{Lin.} \quad (1.4a) \\ \frac{K}{\alpha}\frac{W}{L_{eff}}\gamma_{sat}[(V_{GS} - I_{DS}\frac{R_{DS}}{2} - V_T)^{\alpha}x_{cm} & \text{Sat.} \quad (1.4b) \end{cases}$$

Where x_{cm} is a variable dependent on V_{DS} that incorporates the channel length modulation parameter on the equation, γ_{sat} is the current saturation parameter, L_{eff} is the effective channel length and K (equation 1.5) is provided unit matching by the parameter ζ.

$$K = \mu_{\text{eff}}\,\zeta C_i^{\alpha-1} \tag{1.5}$$

1.2.2 AC Model

1.2.2.1 MOSFET small signal model

The small signal model provides information about the ratio of small perturbations of the large-signal variables. Standard equivalent circuit models for FET devices are well established, being the hybrid-pi model the most used. However, the MOSFET hybrid-pi model does not take into account the contact parasitic resistances that affect TFTs, which may cause some inaccuracies especially in cases of high R_{DS} values.[19]

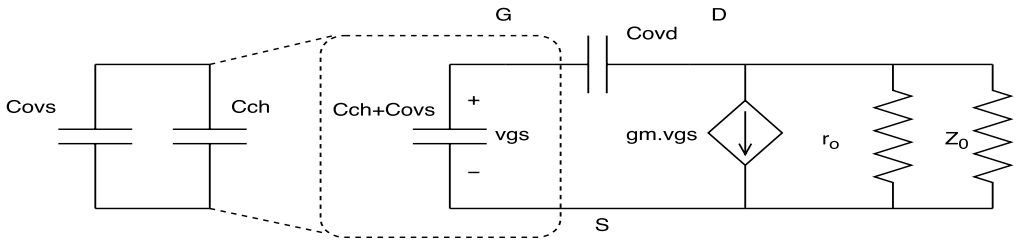


Figure 1.4: FET small signal model circuit for high frequencies

Figure 1.4 displays the MOSFET model adapted for high frequencies with added capacitances, where Covs and Covd are equivalent to the overlap capacities of the source and drain respectively and Cch to the channel capacitance. The term gm stands for the device transconductance and z_0 is in general an arbitrary reference impedance, but usually the characteristic impedance of a line 50 Ω.

1.2.3 S Parameters

The S Parameters (scattering parameters) are a type of high frequency parameters used to describe circuits in terms of wave propagation. They relate incident waves to transmitted and reflected ones, simplifying the circuit analysis. A TFT can be analysed as a 2 port network (Figure 1.5) from which we can obtain the S-parameter matrix (b = S a)[20] and from it extract the S Parameter equations. The physical meaning of S11 is the input reflection coefficient

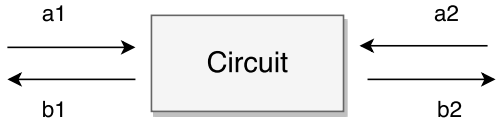


Figure 1.5: Block diagram of a 2-port network
a1 = incident wave (port 1) b1 = reflected wave (port 1)
a2 = incident wave (port 2) b2 = reflected wave (port 2)

with the output of the network terminated by a matched load (a2 = 0). S21 is the forward transmission (from port 1 to port 2), S12 the reverse transmission (from port 2 to port 1) and S22 the output reflection coefficient. [20]

1.2.4 Unity gain cut off frequency

The unity gain cut off frequency (f_T) is the frequency at which the modulus of the short circuit current gain (A_i) is unity (Figure 1.6). It is used as an indicator of the intrinsic speed of a transistor. [21] The expression for the current gain can be obtained by short circuiting the small signal model (Figure 1.4):

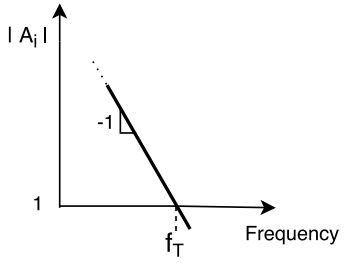


Figure 1.6: Transition frequency of a MOSFET

$$A_i = \frac{I_o}{I_{in}} = \frac{-gm.v_{gs} + sC_{ovd}.v_{gs}}{s(C_{ovd} + C_{ovs} + C_{ch})v_{gs}} = \frac{-gm + sC_{ovd}}{s(C_{ovd} + C_{ovs} + C_{ch})} \tag{1.6}$$

The expression for f_T is then extracted from equation 1.6. When $|A_i| = 1$, and assuming the zero is located at frequencies higher than the cut off frequency, we obtain [22]:

$$f_T \approx \frac{gm}{2\pi(C_{ovd} + C_{ovs} + C_{ch})} \tag{1.7}$$

The main goal of this work is to develop a DC and AC model for a ZTO TFT, as well as obtaining an in depth understanding of physical device modelling techniques and parameter extraction methods. The characterisation and optimization of the model will be carried out through the analysis of the fitting with the measured data.

2

Methodology

2.1 Parameter Extraction Methods

2.1.1 DC Measurement

The devices were measured using a semiconductor parameter analyser (Agilent 4155C) attached to a microprobe station (Cascade M150) in continuous mode with sweeps recorded in ambient conditions inside a Faraday cage. The chosen transistors had varying dimensions, consisting of a channel width of 20 μm and a channel length of 20, 40, 80 and 160 μm, and another device with channel width 160 μm and length 20 μm. In order to remove the shift in V_T, induced by the gate bias stress, several stabilization curves were performed before the measurements were recorded. The optical microscope Olimpus BX51 was used to observe the samples.

2.1.1.1 Threshold Voltage

As mentioned in section 1.1.1, the extraction of the threshold voltage can be difficult for TFT devices. Most V_T extraction methods rely on measurements of the drain current (I_{DS}) and transconductance (gm) versus the gate voltage (V_G) at a low drain voltage. Linear extrapolation techniques and second term order derivatives are two of the examples that may be used in order to find the threshold voltage. The latter calculates the gate voltage at which the second derivative of the current is maximum, taking into account the ideal device model: if $I_{DS} = 0$ for $V_{GS} < V_T$ and starts to increase linearly after $V_{GS} > V_T$ the first derivative will be a step function and the second will exhibit a maximum at $V_{GS}=V_T$. The linear extrapolation technique is simply the value of V_G necessary to make the drain current (linearly extrapolated from the above threshold transfer characteristics) go to zero, with a low applied V_{DS}.[23]

However, the previous methods are based on transfer characteristics and have a dependence on the contact resistance and channel degradation that may lead to erroneous values.[24]The assumption that charge accumulation in the channel increases linearly with V_G above the threshold is not always verified, leading to innacurate result when using linear extrapolation techniques.[25]

2.1.1.2 Contact Resistance

The transmission line measurement (TLM), developed by Shockley, is the most often used method to obtain the resistance in an ohmic contact. It consists on the measurement of the resistance of several devices with varying channel length and fixed W. [26]

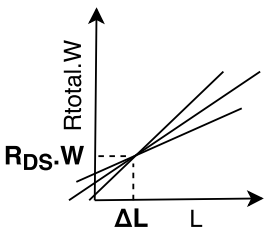


Figure 2.1: Rtot vs L plot for contact resistance extraction method

As the total resistance (R_{tot}) is equal to the sum of the channel resistance (R_{ch}) and the parasitic resistances, mainly the contact resistance (R_{DS}), we can use equation 1.4a to write[18]:

$$R_{\text{tot}}W = \frac{1}{K(V_{GS} - V_T)^{\alpha-1}}(L + \Delta L) + R_{DS}W \tag{2.1}$$

By plotting $R_{\text{tot}}W$ in function of L, and fitting linearly the points with the same V_{GS}, a graphic similar to Figure 2.1 would be obtained.

Ideally, all the lines correspondent to different V_{GS} values would tend to the same point when approaching the limit of a zero-length resistor. The intercept of the lines with the y-axis would then be equal to $R_{DS}W$. But the parameter variation in the devices causes a shift on the position of the intercepts:

- The effective channel length of the device may have a bias dependence causing the intercept points to depend on V_{GS}[27]
- The intercepts may also not occur all in the same point due to errors in the fabrication process that cause the actual channel length of the device to be different from the mask.

So in order to obtain the contact resistance, the slope(m) and intercept(B) values of the $R_{\text{tot}}W$ vs$L$data are extracted using linear fitting. Then B vs m is plotted, where:

$$m = \frac{1}{K(V_{GS} - V_T)^{\alpha-1}} \tag{2.2}$$

$$B = (\frac{1}{K(V_{GS} - V_T)^{\alpha-1}})\Delta L + R_{DS}W \tag{2.3}$$

The value of the contact resistance can be extracted from this plot, as the y-axis intercept corresponds to $R_{DS}W$.

The method has the disadvantage of not providing separate information about the drain and the source contact resistances [28] and assuming the contact resistance is not modulated by any bias. To observe if the contact resistance may exhibit some dependence on the applied gate voltage another method of extraction may be used. To determine the contact resistance and ΔL at a certain V_{GS}, two separate voltages V_{GS}-ΔV_{GS} and V_{GS}+ΔV_{GS} are used (where ΔV_{GS} is an arbitrarily small voltage).[29] The previous used method of the transmission line measurement is then applied for each pair of values, obtaining a solution of contact resistance and ΔL that provides a close approximation for the values at a certain V_{GS}. [29]

2.1.1.3 Power parameter

The power parameter (α) can be extracted from the ($I_{DS} - V_{DS}$) characteristics of the devices. Considering the transconductance expressed as $gm = \frac{\partial I_{DS}}{\partial V_{GS}}$, the expression can be obtained from equation 1.4a [18] :

$$\frac{I_{DSlin}}{gm_{lin}} = \frac{V_{GS} - V_T - \frac{V_{DS}}{2}}{\alpha - 1} \frac{V_{DS}}{V_{DS} - R_{DS}I_{DSlin}} \tag{2.4}$$

By plotting $\frac{I_{DSlin}}{gm_{lin}}$ in function of V_{GS}, we are able to extract α from the slope.

2.1.1.4 Transconductance parameter

The extraction of the transconductance parameter (K) is based on the slope of the $R_{\text{tot}}W$ vs$L$data. The slope m (equation 2.2) raised to $-\frac{1}{\alpha-1}$ is plotted in function of V_{GS}-V_T. The slope of the fit is then equivalent to K raised to $\frac{1}{\alpha-1}$. [18] The mobility value can be obtained from K.

2.1.1.5 Channel length modulation parameter

The channel length modulation parameter (λ) can be obtained by dividing the L_{eff} for the equivalent of the Early Voltage for the TFT (also named V_A). V_A is the absolute value of the intercept of the output characteristics on the V_{DS} axis.[18]

It is incorporated in the model equations by the parameter x_{cm} (equation 2.5):

$$x_{cm} = 1 + \frac{\lambda V_{DS}}{L_{eff}} \tag{2.5}$$

In this equation L_{eff} is the sum of the channel length (L) with the channel length change (gate bias dependent ΔL).

2.1.1.6 Saturation parameter

The saturation parameter (α_{sat}) relates the applied gate bias of the transistor with the saturation voltage V_{DSsat}, the drain voltage at which the transistor enters the saturation region. It can be rewritten as the saturation current parameter (γ_{sat}) by the equation[18]:

$$\gamma_{sat} = 1 - (1 - \alpha_{sat})^{\alpha} \tag{2.6}$$

γ_{sat} can be extracted from the saturation region measurement data. The slope (S) of the fit of ($I_{DS}\frac{L_{eff}}{W}$) to the power of $\frac{1}{\alpha}$ plotted in function of V_{GS} yields[18]:

$$\gamma_{sat} = \frac{\alpha S^{\alpha}}{x_{cm} K} \tag{2.7}$$

2.1.2 Transconductance extraction

The transconductance (gm) is extracted from the partial derivative of I_{DS} with respect to V_{GS} ($\frac{\partial I_{DS}}{\partial V_{GS}}$). It is used in the small-signal model to relate the drain current to V_{GS}.

2.1.3 Capacitance-Voltage Measurement

The extraction of the Capacitance-Voltage (C-V) characteristics was performed using Keysight B1500A and a Cascade EPS150 Triax probe station for the device with a normal gate to source/drain (S/D) C–V configuration, at small signal voltage of 30 mV and frequency f = 10 kHz. The 2-terminal voltage sweep was performed with applied gate voltages from -5 to 10 V, and drain voltage of 0 V with the source open and small signal frequency f = 10 kHz.

2.1.3.1 Dielectric and overlap capacitance

The overlap capacitance (C_{ov}) is composed of the drain overlap capacitance (C_{ovd}) and the source overlap capacitance (C_{ovd}). Assuming the symmetry of the device, C_{ovd} and C_{ovs} are both the same value and equal to $\frac{1}{2}C_{ov}$. We are able to extract the values of these capacitances from the CV curves measured from the device (Figure 2.2 exhibits an example of a CV curve from a TFT). At low V_{GS} the device is in the depletion zone, which causes the channel capacitance to become zero. [30]The gate capacitance is saturated at C_{MIN}, due to the parasitic capacitances of the transistor.

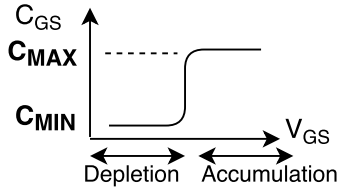


Figure 2.2: Gate-source capacitance example

We can assume C_{MIN} =C_{ov} as the overlap capacitance is the largest of the parasitic capacitances. For higher values of V_{GS} the channel capacitance starts to increase, until saturation occurs at C_{MAX} due to the more dominant response from free carriers provenient from the conduction band.[30]C_i can be extracted from C_{MAX} (equation2.8):

$$C_i = \frac{(C_{MAX} - C_{MIN})}{WL} \tag{2.8}$$

2.1.4 AC Measurement

A Keysight E5061B network analyser with model 10 high frequency probes (6 GHz bandwith) calibrated by a GGB Industries, Inc. CS-11 calibration substrate was used to measure the parameters. The network analyser provided the DC bias from port 1 (connected to the gate of the transistor) whereas the DC bias from port 2 (supplying the transistor drain) was provided through an Agilent 33500B series waveform generator. The network analyser separates the AC small signal input and output from the DC component provided from port 1, but the same does not happen for the DC bias originating from the generator. In order to avoid interfering with the analyser circuitry, a Picosecond 5546 bias tee is used.

The gate was biased at 8 V and the drain at 10 V in order for the TFT to be in saturation. The device chosen for the S parameter analysis had the largest W/L ratio (channel width of 160 μm and a channel length of 20 μm) in order to avoid machine errors related to the minimum current level detected by the apparatus. To further reduce the noise, due to the very small signal, the noise obtained when lifting the probes was removed from the data.

Note: All the measurements were performed both in UCAM and in CENIMAT in different stages of the project.

3

Analysis of Results

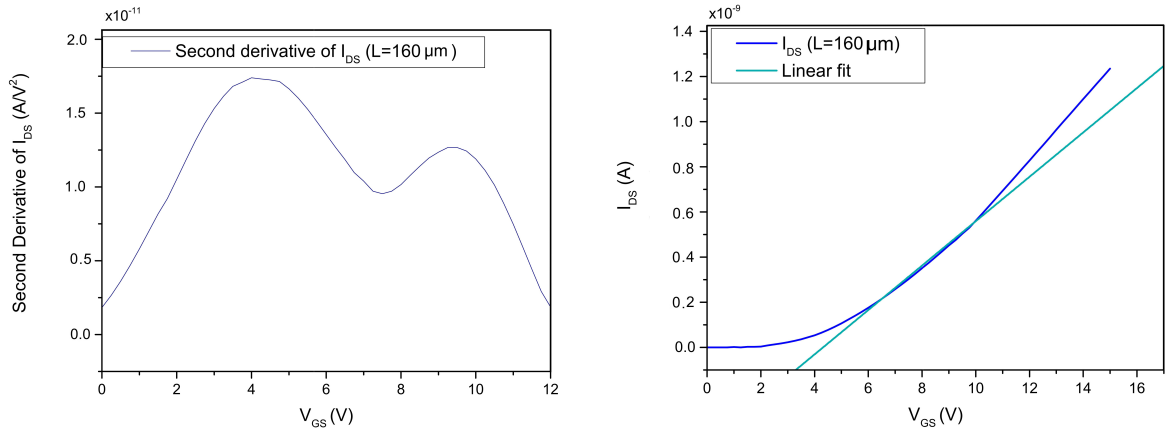
3.1 DC Model

The linear equation parameters were extracted from the transfer curves (V_{DS}=5 mV and a V_{GS} sweep from 0 to 15 V) of four devices with channel width of 20 μm and channel lengths of 20, 40, 80 and 160 μm. The I_{GS} value was also measured in order to analyse the gate leakage. The saturation parameters were extracted from the output characteristic curves (V_{GS} values varying from 6 to 10 V with a 1 V step and a V_{DS} sweep from 0 to 16 V) and the transfer curves (V_{DS}=10 V and a V_{GS} sweep from 0 to 10 V).

3.1.1 Threshold voltage

The second derivative method is highly sensitive to noise, so the use of smoothing functions was necessary in order to obtain a readable result. However, samples have a slow transition from subthreshold to linear phase and using the second derivative method (refered in subchapter 2.1.1.1) still provided results difficult to interpret. The nonlinear behavior around the threshold voltage creates a smooth curve instead of an abrupt peak as we are able to observe in Figure 3.1a. By examining the graphic we are able to estimate the threshold voltage to be around 4 V, but not the exact value. This lead to the choice of linear fitting as the method used for V_T extraction in the first model.

At a relatively low V_G near the threshold voltage, the behaviour is still nonlinear, so those values were excluded. The same occured for very high values of V_{GS}, where the current (and possibly charge accumulation in the channel) does not increases linearly with V_G even at the very low applied V_{DS}. The fitting was performed for the interval of 6 to 12 V (Figure 3.1b), as the value for V_T had been roughly estimated to be 4 V. The same procedure was repeated for the remaining transistors, and the results were similar for all the dimensions (table 3.2 exhibits the extracted V_T values).

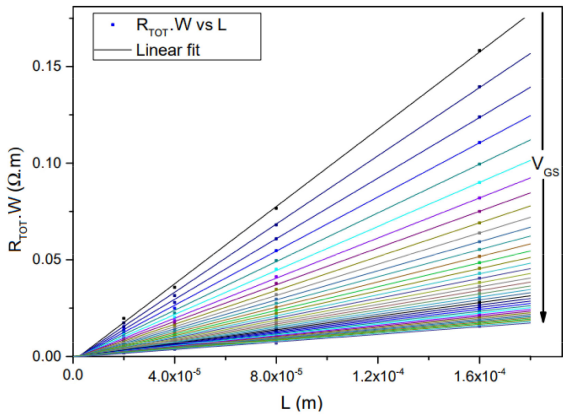


(a) Plot of Second derivative of I_{DS} vs V_{GS} for transistor with 20/160 ratio

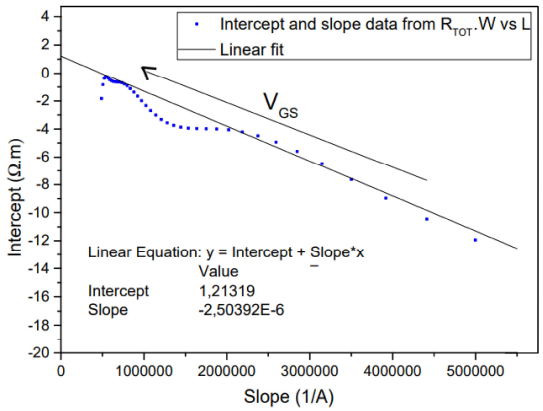
(b) Plot of I_{DS} vs V_{GS} with applied V_{DS}=5 mV and linear fitting for transistor with 20/160 ratio

Figure 3.1: Methods of threshold voltage extraction

3.1.2 Contact resistance



(a) Plot and linear fitting of R_{tot}.W vs L data for various values of V_{GS}-V_T (from 1 to 10 V with 0.1 V intervals)



(b) Linear fitting of Intercept vs Slope data from R_{tot}.W vs L

Figure 3.2: Contact resistance extraction

The contact resistance was extracted from the transfer curves of transistors with four different channel lengths at low applied V_{DS} (5 mV). The R_{tot} values were obtained by dividing the applied V_{DS} by the drain current measurements. Following the contact resistance TLM extraction procedure (described in section 2.1.1.2) results in various values of intersections (Figure 3.2a).

In order to obtain a R_{DS} value the slope (m) and intercept (B) values of the fitted R_{tot}W vs L data were plotted (Figure 3.2b). The R_{DS}W value obtained was of approximately 1.2 Ωm which is equivalent of a contact resistance of 60 000 Ω for a transistor with a channel width of 20 μm. From this data we are also able to extract the effective channel length.The average L value for all the intersections of R_{tot}.W vs L linear fit was -1 μm, which is the value for ΔL according to equation 2.1.

3.1.3 Power parameter

The power parameter was extracted for values of V_{GS} higher than the threshold voltage (V_{GS}-V_T>1) to minimize the contact resistance error. The method described in section 2.1.1.3 was performed (Figure 3.3), using the data from a transistor with dimensions W=20 μm and L=40 μm. The values of $\frac{I_{DSlin}}{gm_{lin}}$ for applied V_{DS} of 5 mV were plotted in function of V_{GS}-V_T, and the slope obtained through a linear fitting.

The value of α used in the model was 2.26, as the slope value was approximately 0.796.

3.1.4 Transconductance parameter

The slope values of the R_{tot}.W vs L data (obtained previously when extracting the contact resistance) were raised to $\frac{1}{1.26}$ and then plotted in function of V_{GS}-V_T (Figure 3.4).

The fitted line had a slope of approximately 2.75×10^{-6} and intercept of 1.2×10^{-7}. The obtained K value was of 1×10^{-7} $FV^{-1}s^{-1}cm^{-1}$ as the value of α is 2.26.

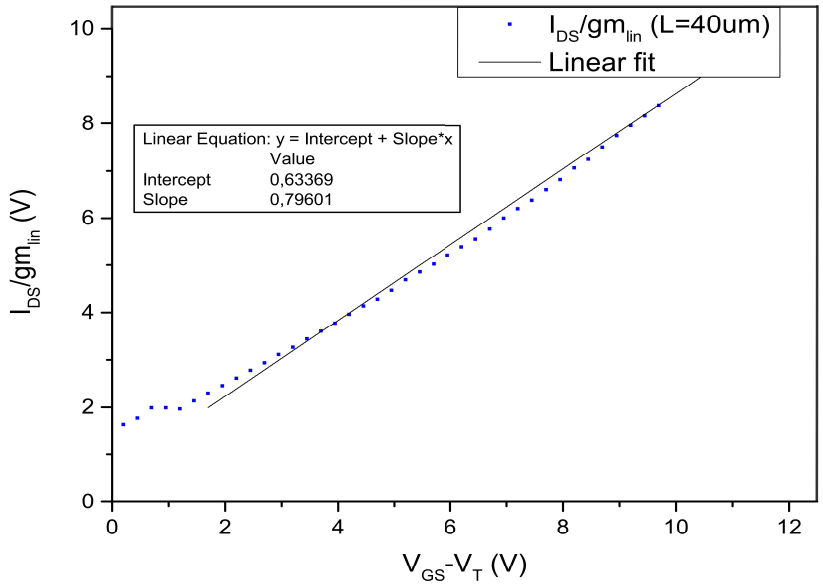


Figure 3.3: Linear fitting of I_{DS}/gm_{lin} versus V_{GS}-V_T for a transistor with dimensions W=20 μm and L=40 μm

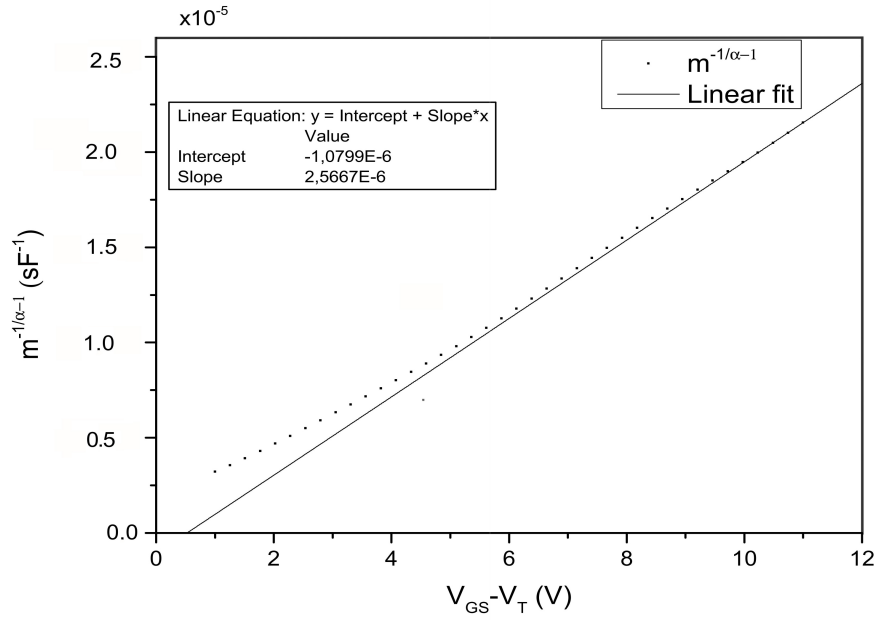


Figure 3.4: Linear fitting of m to the power of $-\frac{1}{\alpha-1}$ in function of V_{GS}-V_T

3.1.5 Channel length modulation parameter

V_A extraction was performed for V_{DS} values above 13 V. In this way the fitting was always performed on the saturation region, regardless of the applied value of V_{GS} (varied between 5 and 15 V).

The average of the obtained $|V_A|$ values (table 3.1) was calculated (excluding the more dissimilar values), resulting in the value of 1842 V, which yielded a λ value of 1.09×10^{-8}m/V.

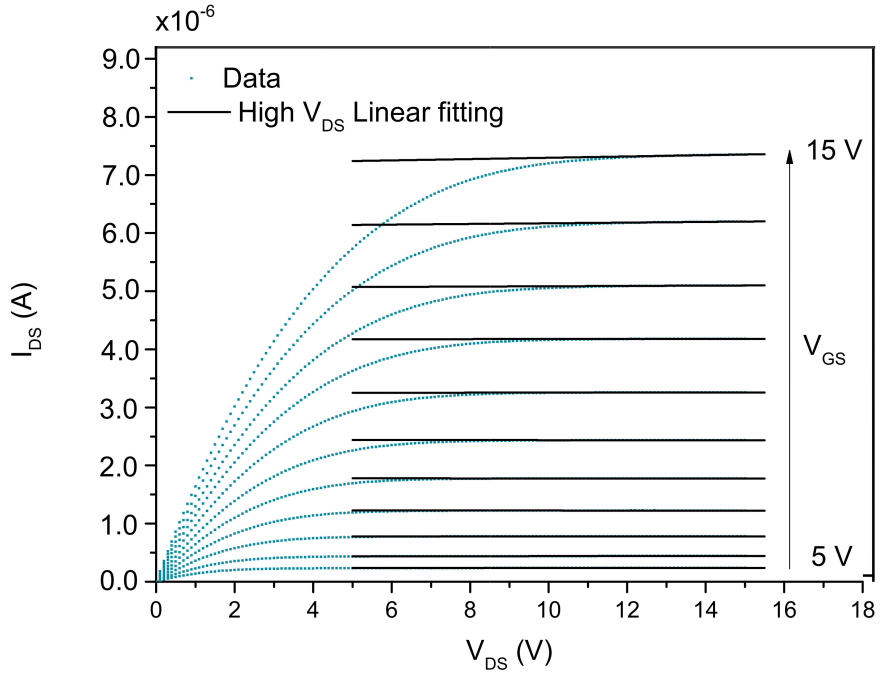


Figure 3.5: Linear fitting of saturation region for the output curves of a transistor with dimensions W and L equal to 20 μm

Table 3.1: Obtained V_A values for all the applied V_{GS} curves

V_{GS}(V)	5	6	7	8	9	10	11	12	13	14	15
$\lvert V_A \rvert$ (V)	802	1458	13804	4954	13759	5022	2215	1044	528	347	215

3.1.6 Saturation parameter

The transistor with the longest channel length (L=160μm) was used in order to reduce contact resistance effects. The plot of $(I_{DS}\frac{L_{eff}}{W})$ to the power of $\frac{1}{\alpha}$ in function of V_{GS} was linearly fitted (Figure 3.6) and the slope value extracted. The γ_{sat} value obtained was of 0.63, as the slope value was approximately S=4.6×10^{-4} A$^{\frac{1}{\alpha}}$.

3.1.7 Model fitting

The parameters used for the linear fitting are summarized in table 3.2, and were used in equation 1.4a in order to obtain the model linear transfer curve (Figure 3.7).The γ_{sat} value was slightly altered to improve the continuity of the model.

The equation 1.4a was used for the transfer curve linear fitting. For the output curves fitting, equations 1.4a and 1.4b were altered and a transition function was added in order to obtain a better modeling of the transition region (equations 3.1a and 3.1b).

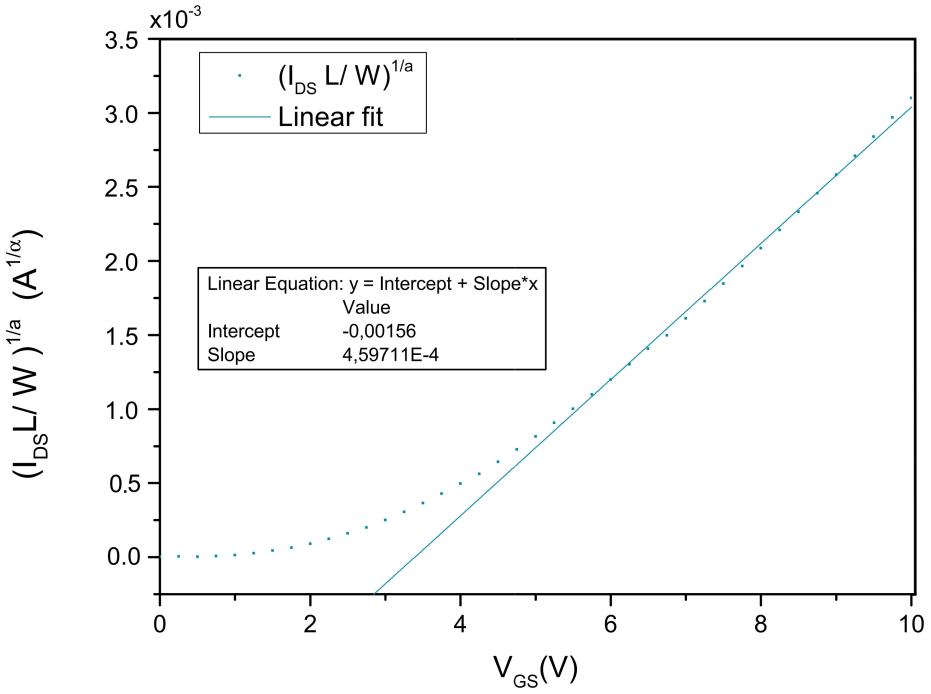


Figure 3.6: Linear fitting of $(I_{DSlin}\frac{L}{W})^{\frac{1}{\alpha}}$ in function of V_{GS} for a transistor with dimensions W=20 μm ans L=160 μm

Table 3.2: Extracted parameters summary.

Transistor Length (μm)	V_T (V)	**Contact Resistance** (Ω)	Δ**L** (μm)	α	**K** (F/V.s)	λ (μm/V)	γ_{sat}
20	3.8						
40	3.8	60 000	1	2.26	1×10^{-7}	0.01	1.023
80	4.5						
160	4.3						

$$I_{DS} = \begin{cases} K\frac{W}{L}(V_{GS}-V_T-\frac{V_{DS}}{2})^{\alpha-1}(V_{DS}-I_{DS}R_{DS}-(1-\frac{1}{\alpha})(V_{DSint}-I_{DS}R_{DS})^{\alpha} & \text{Lin.(3.1a)} \\ \frac{K}{\alpha}\frac{W}{L}\gamma_{sat}[(V_{GS}-I_{DS}\frac{R_{DS}}{2}-V_T)^{\alpha}x_{cm} & \text{Sat.(3.1b)} \end{cases}$$

Where V_{DSint}=$(V_{DS}^{-m}+(V_{GS}-V_T)^{-m}))^{\frac{-1}{m}}$. The parameter m is an adjustment parameter related to the sharpness of the knee region. The plotted model is depicted in Figures 3.7 and 3.8.

The fit is best in the region from which the threshold voltage was extracted (approximately 6 to 12 V). Above a certain value of V_{GS} we observe an increase on the measured drain current and transconductance, which are not reproduced by the model.

Possible reasons for the obtained fitting were mentioned in section 2.1.1.2, and relate to the method of contact resistance extraction. The mobility extraction could also be a possible source

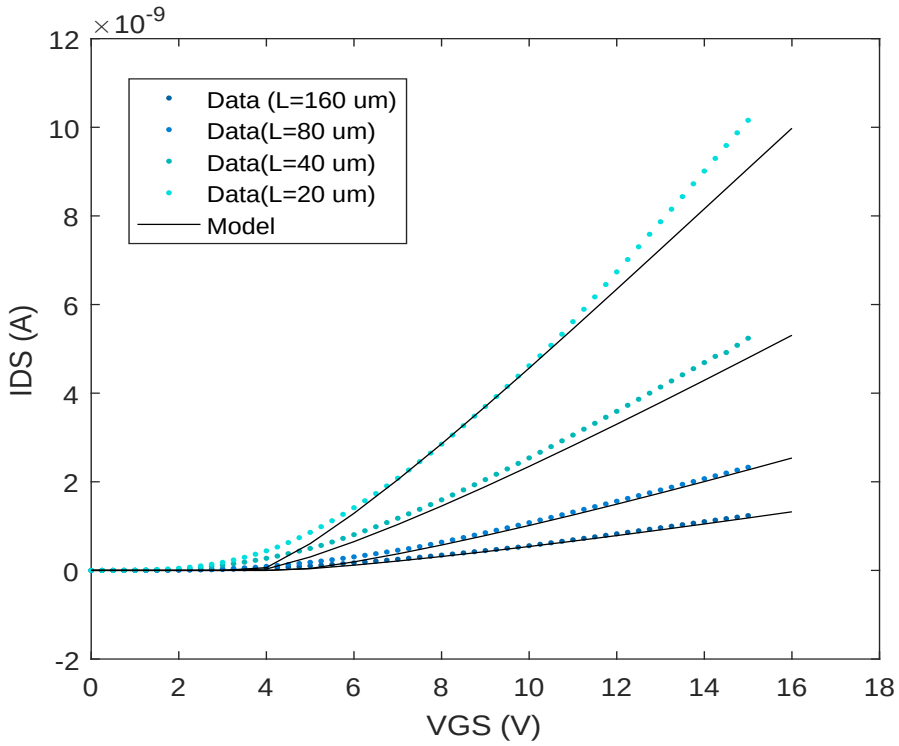


Figure 3.7: Linear fitting of model with VGS dependent contact resistance and ΔL for applied VDS of 5 mV

of error, as the effective mobility is a difficult value to extract, depending on the values of other extracted parameters such as V_T. The output curves for V_{GS} values from 8 to 12 V are depicted in Figure 3.8. The modelled output curves fail to simulate the transistor behaviour, fitting only for the values of 9 and 10 V.

3.1.8 Bias dependent parameters

In order to improve the poor model fit several measures were taken, such as investigating the possibility of channel length fabrication errors, and bias dependence of the parameters that was not taken into account. The threshold voltage was extracted from the transfer curves (V_{DS}=100 mV and a V_{GS} sweep from 0 to 18 V) of three devices with channel width of 20μm and channel lengths of 40, 80 and 160 μm. The V_{DS} was slightly increased but the device was still operating in the linear region. The objective was to increase the current value and reduce the noise that could affect the extraction of parameters. The device with channel length of 20 μm was excluded so as to minimize contact resistance effects.

The samples were analysed using an optical microscope, where the channel length was measured and compared with the mask channel length. It was concluded that the physical length did not differ significantly from the mask dimensions (C). The effective channel length was then tested, as it can suffer from a bias dependency [31] which could be significant enough to influence the fit. A different extraction method for the contact resistance and effective channel length (referred in chapter 2.1.1.2) was used. The extraction procedure is quite similar to the one previously performed, except applied to a pair of values varying 0.03 V (the value of ΔV_{GS}) from the V_{GS} the contact resistance solution is being extracted.

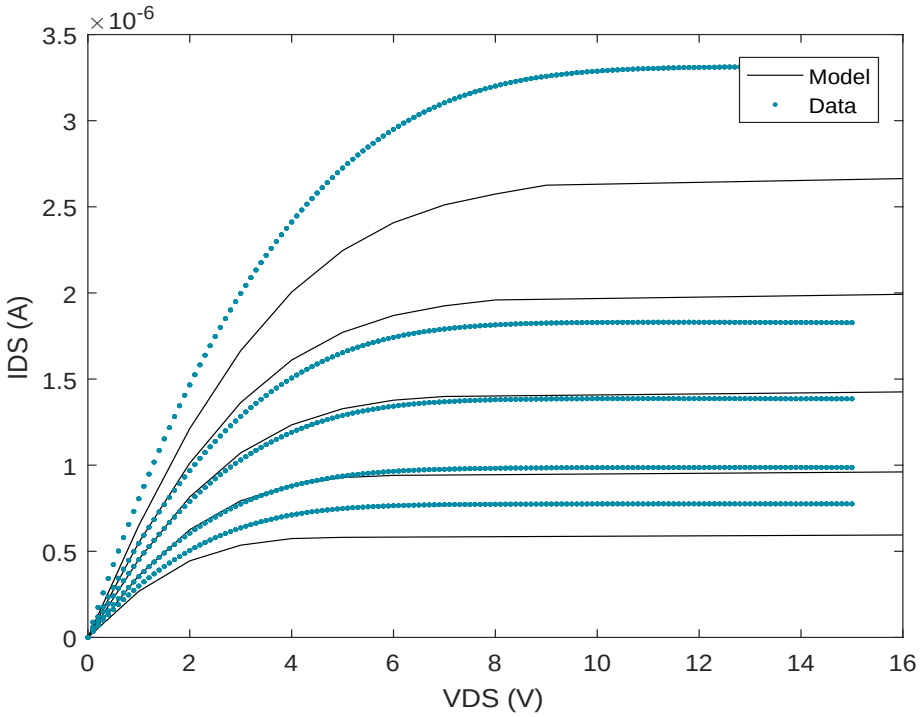


Figure 3.8: Linear fitting of model with V_{GS} dependent contact resistance and ΔL for applied V_{DS} of 10 V

From it the results from table 3.3 were obtained.

Table 3.3: Extracted parameters summary.

V_{GS}-V_T **(V)**	**Contact Resistance . W (Ω.m)**	**ΔL(μm)**
1	2.80	-0.56
2	1.21	-1.26
3	1.26	-1.22
4	1.21	-1.27
5	0.84	-1.68
6	0.66	-1.92
7	0.35	-2.42
Average value	1.19	-1.47

The extracted contact resistance exhibits bias dependency as the value appear to decrease with increasing gate bias. The same is verified for the extracted ΔL values, which decrease with applied V_{GS} meaning that the effective length decreases with gate bias.

The average value (1.19 Ω.m) means that for these transistors of 20 μm width the contact resistance would be 59 500 Ω, very similar to the value extracted for the first model fit (of 60

000 Ω). But if the contact resistance bias theory is correct, it varies from 17 500 Ω to values higher than 100 000 Ω. This may be the explanation for some discrepancies on the the first model fitting.

Table 3.4: Extracted parameters summary.

Transistor Length (μm)	**Vt (V)**	**Alpha**	**K (F/V.s)**	**λ(μm/V)**	**γ_{sat}**
40	5				
80	6	2.55	4.5×10^{-8}	8.89×10^{-8}	1.19
160	6				

The remaining parameters were extracted by the same methods previously used (in subchapters 3.1.3, 3.1.4, 3.1.5 and 3.1.6). Table 3.4 exhibits the extracted values for the parameters.

3.1.9 Second Model fitting

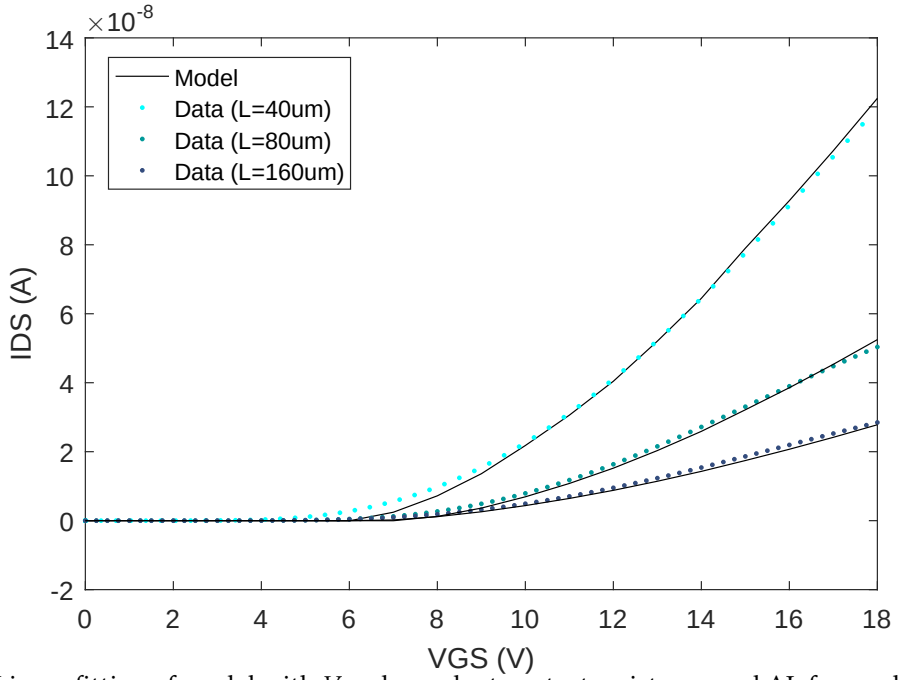


Figure 3.9: Linear fitting of model with V_{GS} dependent contact resistance and ΔL for applied V_{DS} of 100 mV

Using the variable contact resistance values it was possible to improve the fitting of the model. The model fit the measured transfer curve of the transistor even at higher values of V_{GS}, behaving better than the first model. The region near the threshold was not as effectively modelled, however the transistor does not behave as linearly in that region so the worse fit was expected. The model did not achieve a reasonable result for the saturation region (Figure 3.10). The effective mobility value could be the responsible for the fit, as the extraction method depends on the values of V_T and is sensitive to contact resistance, and therefore disposed to errors. We observe that the scaling of model curves is higher than the data, and there is an

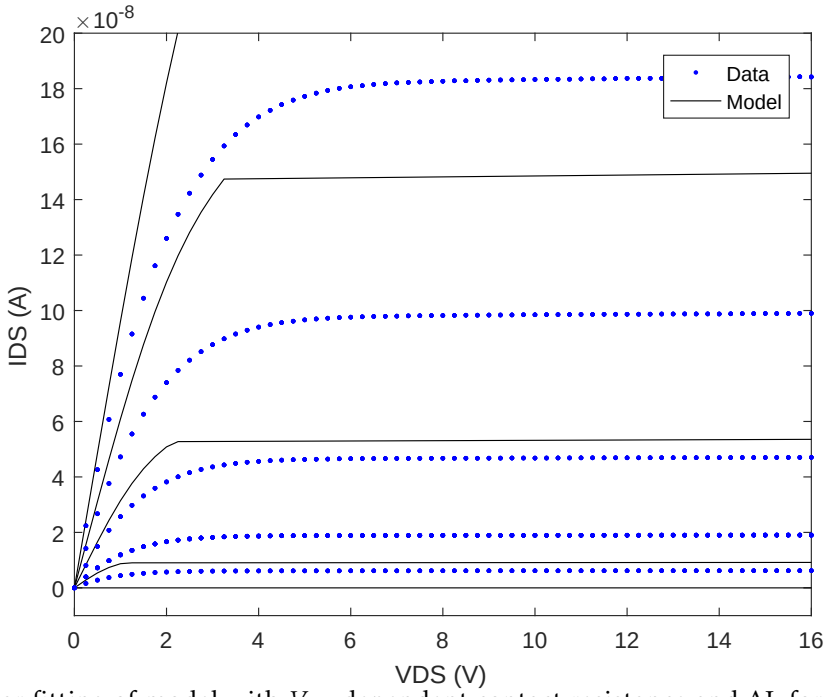


Figure 3.10: Linear fitting of model with V_{GS} dependent contact resistance and ΔL for applied V_{DS} of 100 mV

overestimation of the drain current. A better fitting can be obtained when scaling the model by $\frac{1}{2}$ (Figure 3.11). This could indicate errors with the power and transconductance parameters, which are related to the transistor's mobility.

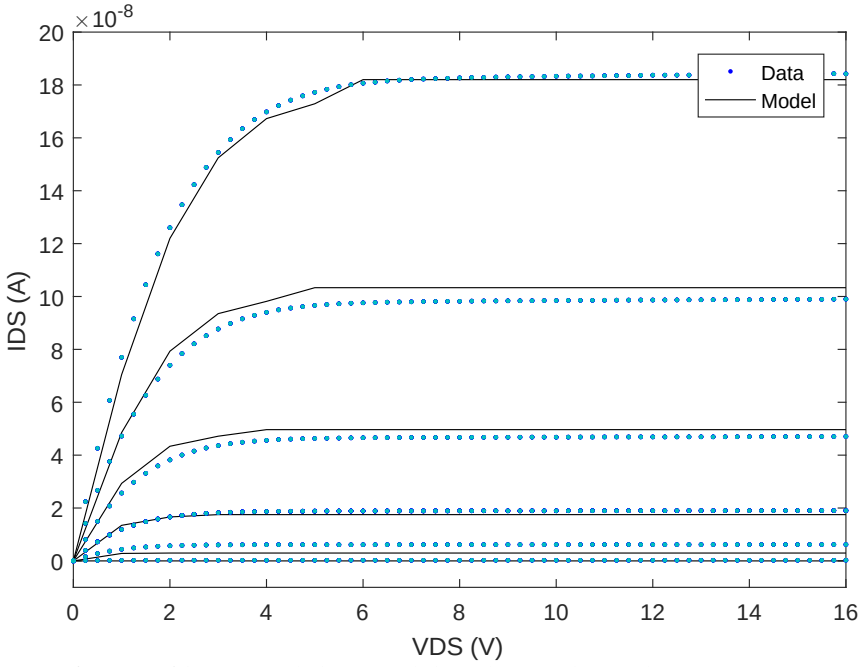


Figure 3.11: Linear fitting of lower mobility model with V_{GS} dependent contact resistance and ΔL for applied V_{DS} of 100 mV

In order to analyse the fitting of the output curve, the saturation mobility was calculated,

using the formula expressed in equation 3.2[32].

$$\mu_{sat} = \frac{\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2}{\frac{1}{2}C_i\frac{W}{L}} \tag{3.2}$$

The objective was to compare the value of the effective mobility to the saturation mobility and see if the difference was very significant, indicating that the effective mobility could have extraction errors. The transfer curve for the transistor with W=20μm and L=80μm with an applied V_{DS} of 10 V was used, obtaining the plot depicted in Figure 3.12. We are able to

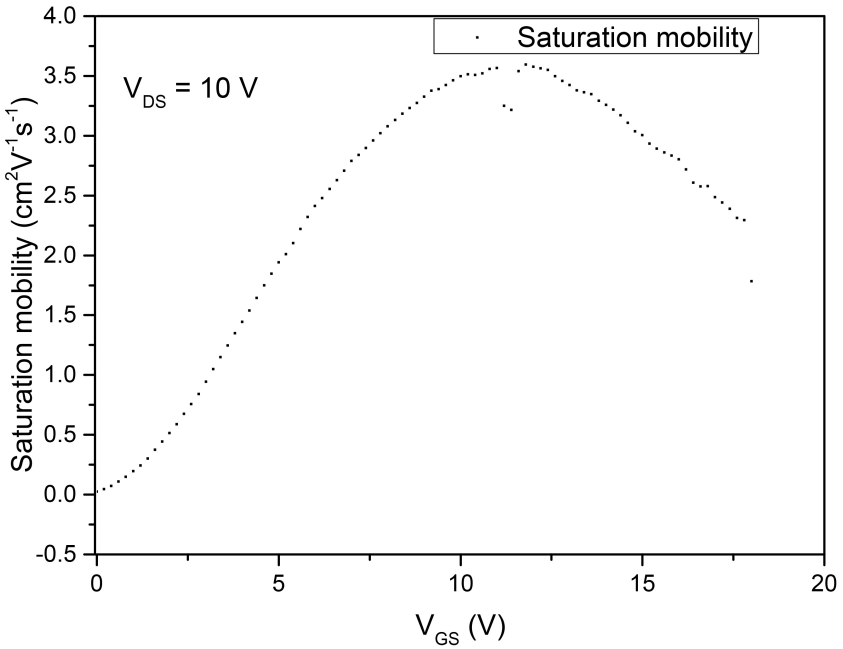


Figure 3.12: Plot of saturation mobility versus V_{GS} for a transistor with W=20μm and L=80μm with an applied V_{DS} of 10 V

observe that the mobility value increases with applied V_{GS} until approximately 10 V, but for higher V_{GS} values the mobility starts to decrease. The highest mobility value is 3.7 $cm^2V^{-1}s^{-1}$, that results in a K of approximately 1.4×10^{-7} F/V.s. This value is higher than the extracted beforehand, so there is a significant difference in the values of mobility in the model and data, which influences the values of the parameters that depend on that extraction. Therefore another method for the extraction of the effective mobility should be used on these devices.

3.2 AC Model

3.2.1 Transconductance

In order to obtain the device transconductance for the small signal model, the first derivative of the drain current in function of V_{GS} was plotted (Figure 3.13). This value is normally constant in the saturation region as the change in drain current is not as noticeable, however that was not the case for the obtained values as it continued to increase. The gm value for the bias point conditions (V_{DS}=10 V and V_{GS}=8 V) is of approximately 4×10^{-6} $\frac{1}{\Omega}$.

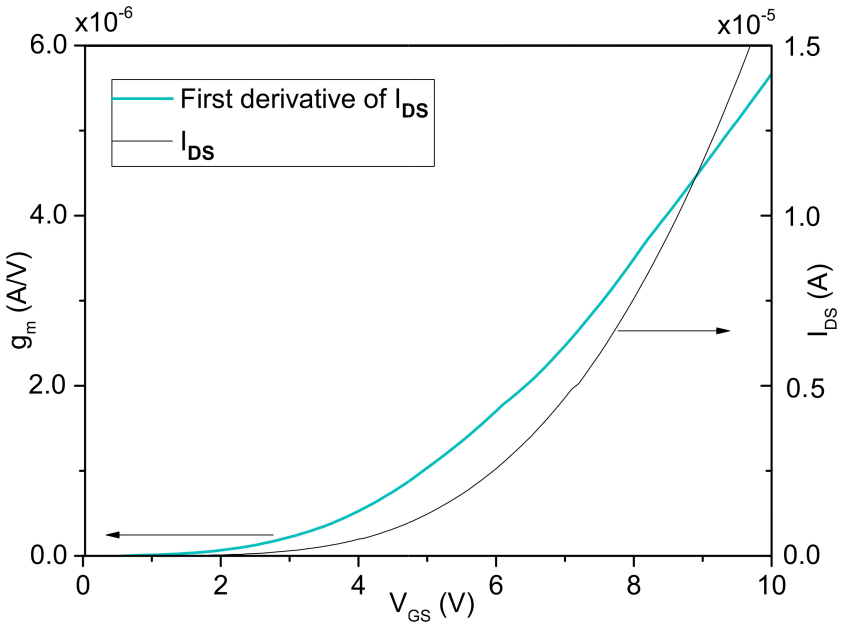


Figure 3.13: I_{DS} and first derivative of I_{DS} in function of V_{GS} with applied V_{DS} of 10 V for gm extraction

3.2.2 Dielectric and overlap capacitance

The values of capacitance in function of gate-source voltage were extracted for the transistor with dimensions W=160 μm and L=20 μm(Figure 3.14). The measurements were repeated and the average of the values obtained. The value of C_{MIN} obtained was of 6×10^{-13}F which can be divided in order to obtain the source and drain overlap capacitances. The average value of C_{MAX} was 1.9×10^{-12} F so the Cch (gate capacitance) value calculated to be of 1.3×10^{-12}F.

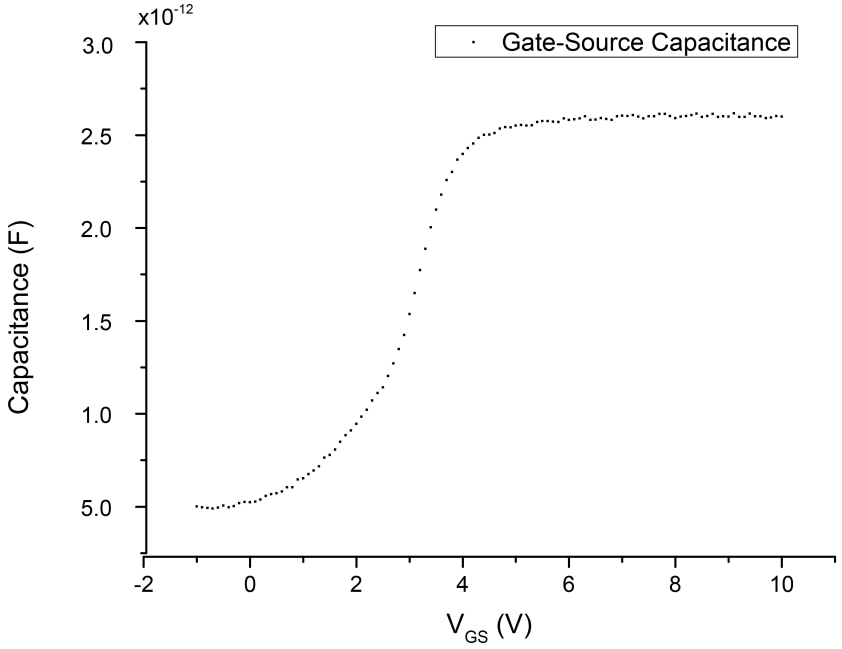


Figure 3.14: Capacitance measurement for transistor with dimension 160/20 μm

The summary of extracted capacities and transconductance of the device can be found on table 3.5. As the gate capacitance value is known, we are able to obtain the gate capacitance per

unit of area C_i, which is 40.62 nF/cm^2.

Table 3.5: High frequency parameters summary.

Gate capacitance (F)	Overlap capacitance (F)	$g_0(1/\Omega)$	gm$(1/\Omega)$
1.3×10^{-12}	3×10^{-13}	$1/50$	4×10^{-6}

3.2.3 S parameters fitting

The S parameters were measured from a frequency of 1 kHz to 1 GHz. The TFT was biased at V_G=8 V and V_D=10 V in order to be in the saturation region and obtain a good performance. The fitting for the S_{11}, S_{21}, S_{22} parameters was performed with the equations obtained from the small signal model (Appendix A) and the h_{21} with equation 1.6.

3.2.3.1 S_{11}

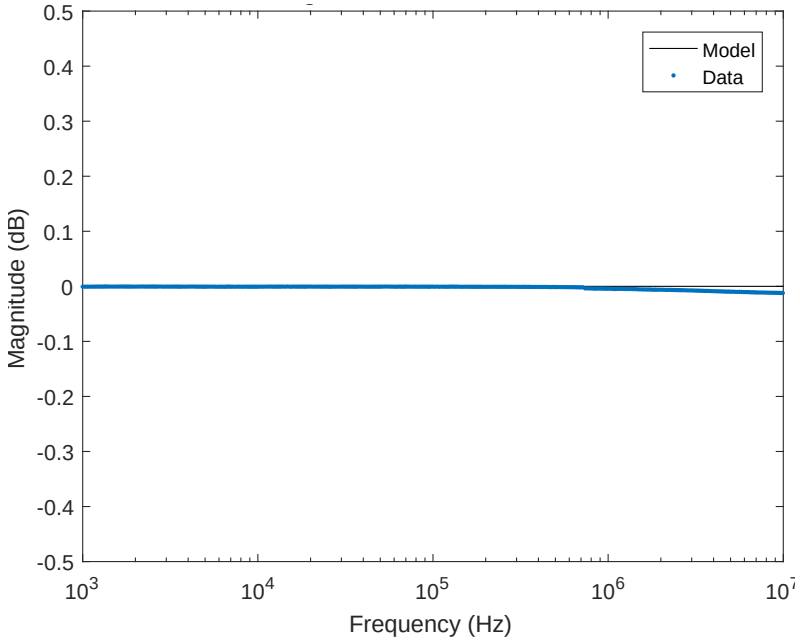


Figure 3.15: Fitting of S_{11} magnitude

The S_{11} was the parameter that was most affected by low frequency noise. As the value is very close to 0 dB, any oscillations may influence greatly its value and the value of the obtained current gain. The fitting of the S_{11} magnitude is good until the frequency of 50 MHz, where the data starts to exhibit a drop and the model stays constant. This difference is exarcerbated with the increase of the frequency as the model only starts to drop at frequencies above 100 MHz. However, as the cutoff frequency of the device is lower than 50 MHz (f_T is 1 MHz as it will be discussed later in section 3.2.4), the fitting for the operating frequencies is acceptable, with the model having a very small relative mean square error of 0.12 for the total measured frequency range, and 15μ for the working frequencies under f_T. The relative mean square error

was calculated from equation 3.3:

$$rMSE = \frac{1}{n}\sum_{t=1}^{n}(\hat{Y}_i - Y_i)^2 \tag{3.3}$$

Where n is the number of data points, $\hat{Y}_i$ the prediction values vector and Y_i the measured values vector.

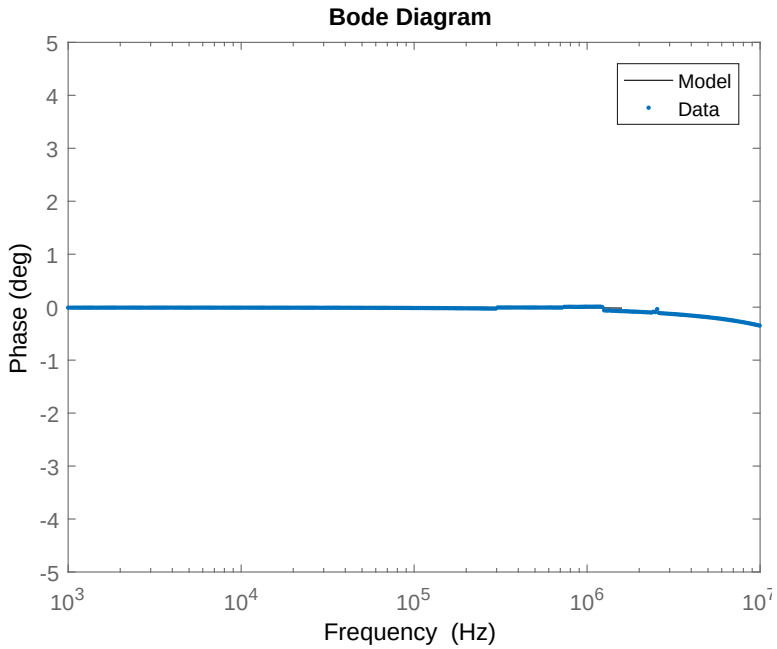
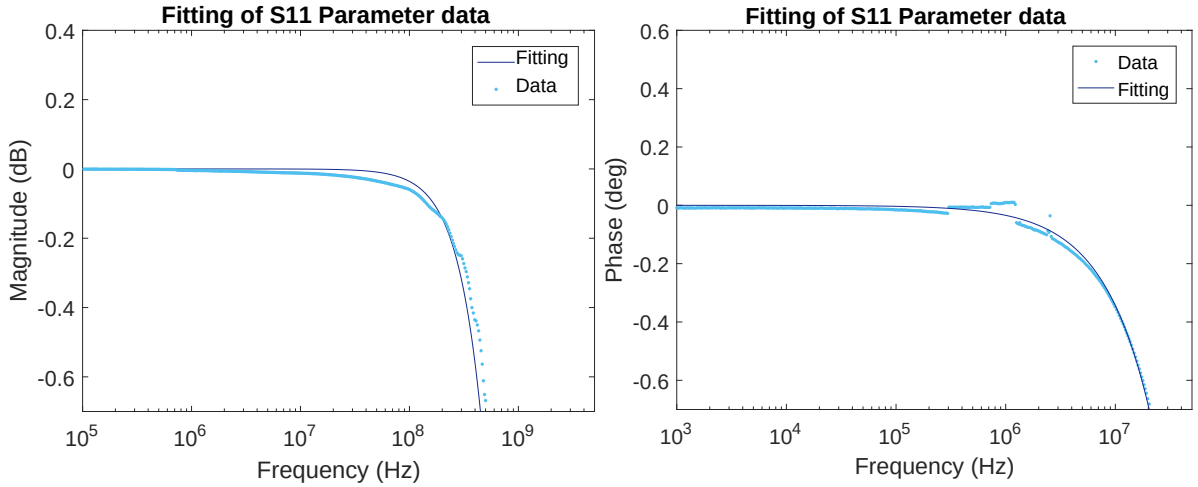


Figure 3.16: Fitting of S_{11} phase

The same is observed for the S_{11} phase (Figure 3.16, with the model not fitting as well for higher frequencies above the cutoff where the data exhibits a drop.



(a) Fitting of S_{11} magnitude with function **(b)** Fitting of S_{11} phase with function

Figure 3.17: Fitting of S_{11} data with function

Some discontinuities exist in the S_{11} parameter data, that can cause errors when obtaining the device's current gain. This occurred when removing the measurement noise due to the very

low value of the parameter. As the model being used is the MOSFET, the presumption of there being only one influential pole at low frequencies in the S_{11} parameter is valid. Taking that assumption into account, in order to reduce the noise caused by the measurement a function was used to fit the extracted data:

$$H(s) = \frac{A}{Bs+1} \tag{3.4}$$

The obtained values for the constants were A=1 and B=6×10^{-10}, which signifies that the pole would be located at approximately 2.7×10^{7} Hz.

It is possible to observe in figures 3.17a and 3.17b that although the fitting does remove the discontinuities that could have caused errors in the calculation of the current gain, it does not completely translate the S_{11} parameter. There is a slight magnitude drop that occurs on the data and not on the fitting. The cause may lay in the assumption that only one pole is present at lower frequencies, and indicates that the MOSFET model is too simplistic to explain the TFT high frequency behaviour.

3.2.3.2 S_{21}

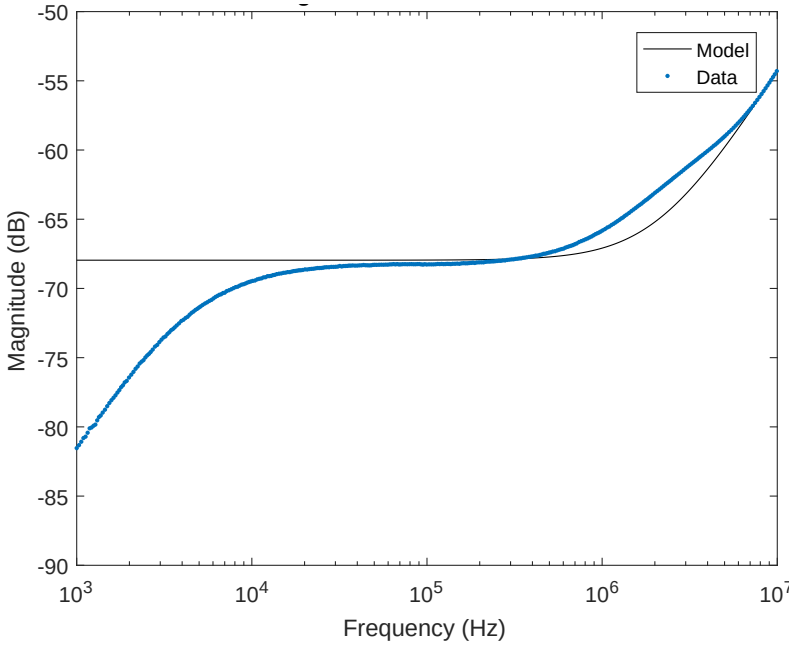


Figure 3.18: Fitting of S_{21} magnitude

The S_{21} model only fits the data for frequencies above 10 kHz. For lower frequencies the MOSFET model tends to the value $-\frac{2gm}{g_0}$ (obtained from equation A.5 when s tends to zero). The value of g_m can be assumed correct, as the model and the data coincide at lower frequencies between 10 kHz and 1 MHz. However the measured data magnitude at low frequencies is not constant, but increases with the frequency until a constant value is met at approximately 10 kHz, meaning that at least an extra zero and pole exist at lower frequencies that were not described in the model.

For frequencies above 1 MHz the fitting error increases with the frequency. This is observed in Figure 3.19 as the data phase suffers from noise at higher frequencies.The error for the S21

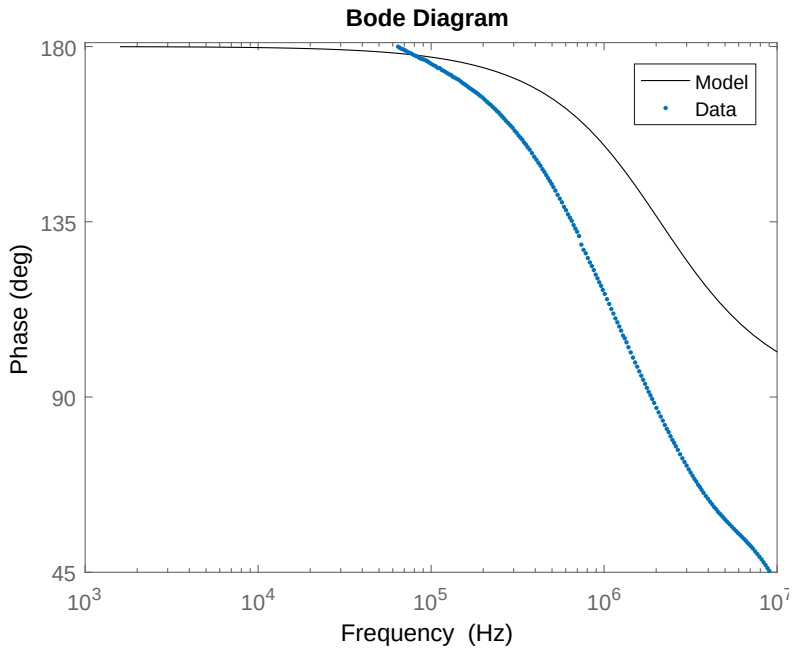


Figure 3.19: Fitting of S_{21} phase

fitting is of 9.9, a higher value than S_{11} that indicates the fitting deviates from the data. If only considering the frequencies lower than f_T the error is even higher, of 17.8.

3.2.3.3 S_{22}

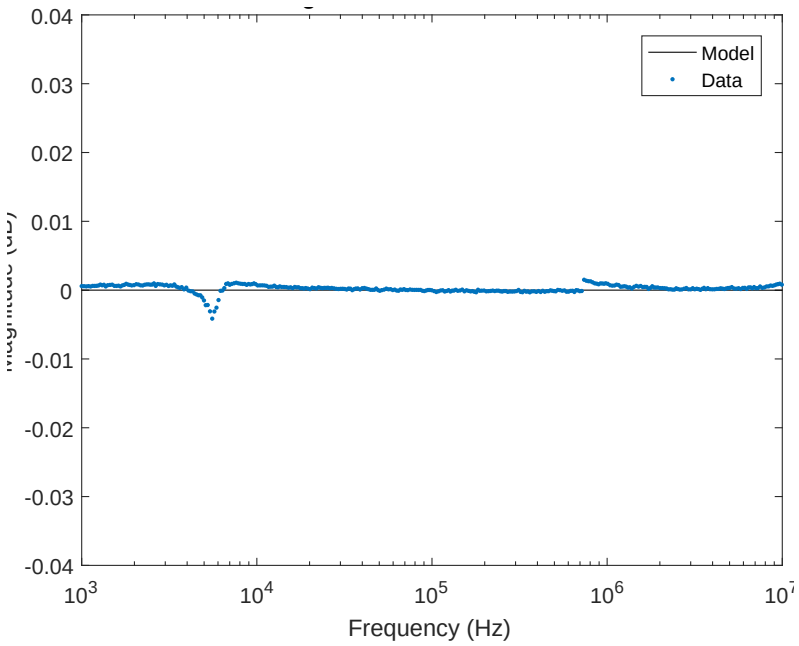


Figure 3.20: Fitting of S_{22} magnitude

The S_{22} parameter is zero dB at low frequencies, exhibiting only some noise variations that slightly alter this value. as the value is so reduced, the measured data noise causes a higher error than the other fittings, of 24.8. If the measuring noise is ignored, the model appears to describes well the TFT for all the operating frequencies and until the frequency of 20 MHz.

Above that value, the data starts to exhibit some degradation that is not observed in the model.

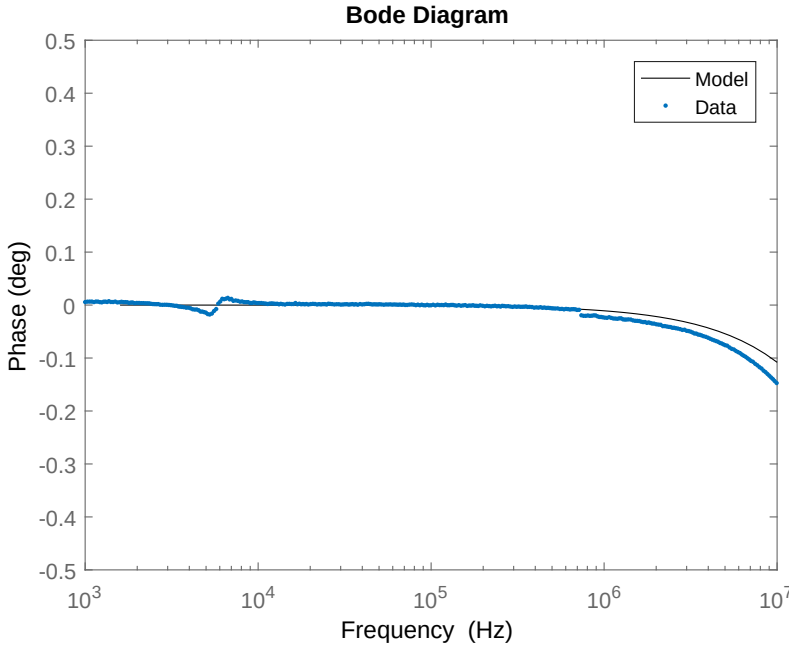


Figure 3.21: Fitting of S_{22} phase

The same is observed for the S_{22} parameter phase, as only above a high frequency (higher than the cutoff frequency) we observe a significant deviation from the measurements.

3.2.4 Current Gain

The h_{21} equation was obtained from the small signal model (equation 1.6) and the extracted parameters applied. The intrinsic current gain was derived from the measured S parameters, using the equation A.8 (presented in appendix 1), and plotted with the model expression (Figure 3.22). We can observe that for frequencies above 10 kHz the current gain decays with increasing frequency as it is expected for a field effect transistor, following the $\frac{1}{f}$ (-20 dB/decade) slope. There is a discrepancy between the model and data, as the model exhibits the same behaviour at a slightly lower magnitude value for frequencies above 10 kHz. Between 1 kHz and 10 kHz there is a notable difference: the model displays the same slope value and the slope of the data varies. We can presume the cause to be the existence of an extra pole that is not described on the model at the measured frequencies. The parasitic resistances and their connections vary and affect the device in a significant way, creating poles and zeros that are most likely the reason why the MOSFET model could not adapt to the TFT.

The f_T for the TFT was found to be about 1 MHz, differing from the model which predicted the lower value of 0.7 MHz. We can analyse the current gain in order to understand what which S parameter had more influence the fitting. We are able to rewrite equation A.8 as [22]:

$$h_{21} = \left| \frac{S_{21}}{(S_{11}-1)(S_{22}+1)} \right| \tag{3.5}$$

The term $S_{21}S_{12}$ is small as most of the power is reflected and not transmitted. According to the experiments the $(1-S_{11})(1+S_{22})$ term is significantly larger, and dominates over $S_{21}S_{12}$ (Figure

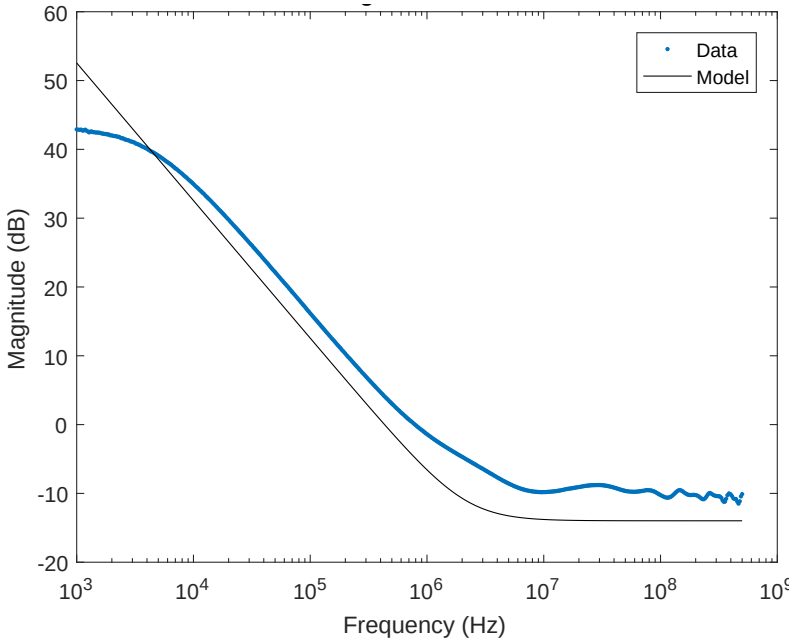
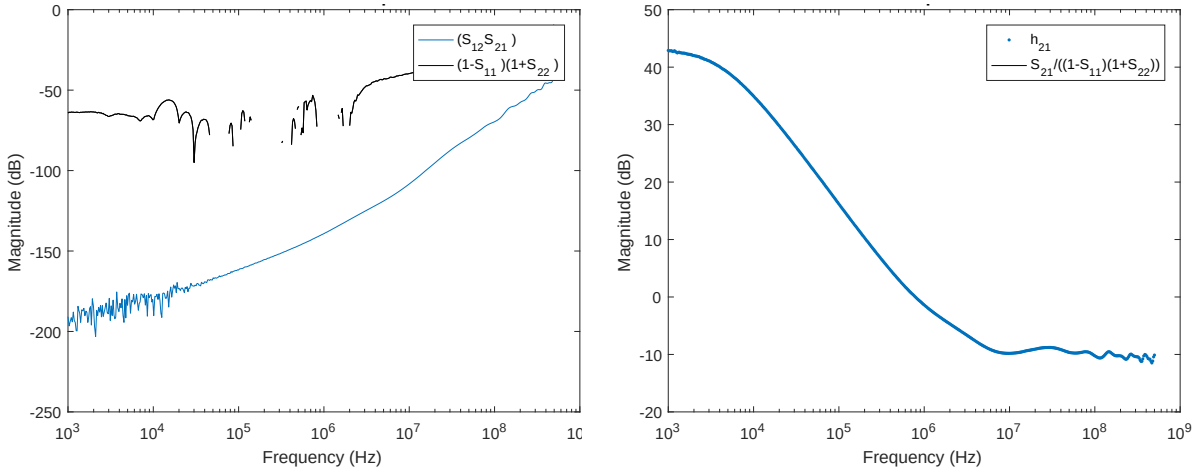


Figure 3.22: Fitting of h_{21}

3.23a) . The denominator can be approximated to be $(1 - S_{11})(1 + S_{22})$, as the approximation coincides with the parameter (Figure 3.23b).



(a) Plot of $S_{21}S_{12}$ and $(1 - S_{11})(1 + S_{22})$ **(b)** Comparison of h_{21} parameter with approximation

Figure 3.23: h_{21} approximation comparisons

As the error from parameter S_{11} is small, the h_{21} fitting error is caused mainly due to parameter S_{21} and S_{22}. This raises the question of the fitting error being partially caused due to machine noise which could alter significantly the low value of S_{22}. The errors caused by S_{21} however are visibly due to lacking components in the traditional MOSFET model, whose connections create zeros and poles not described in the model's equations when applied to a TFT.

4

Conclusion and future perspectives

The process of extraction of parameters, albeit being a very important part of the modelling process, is difficult to perform correctly in new devices on which the physical phenomena is not completely understood. This may result in many possible errors due to lack of accuracy of the extracted parameters and reliability of the chosen extraction methods. However, is during the extraction of parameters that we may perceive physical properties and gain insight on the device behaviour depending on which methodology best fits the data. The threshold voltage, turn-on voltage, power parameter and transconductance parameters were extracted in a ZTO TFT. The extraction of effective channel length and parasitic series resistance was also performed, determining that the bias dependency of these parameters should not be disregarded for this device. From the results we are able to conclude that the effective channel length is smaller than the physical. We are also able to observe that the contact resistance decreases with the applied gate bias, contrary to the effective channel length which increases in module.

A modelling prediction for the linear regime of a ZTO thin film transistor with good agreement with the experimental result was obtained. The model is validated by comparing with measurements of three different transistors (with channel lengths of 40, 80 and 160 μm). The model is not as good at predicting the transistor behaviour in the saturation regime, which was expected due to the parameter extraction methods not taking into account the possibility of significant variation in the contact resistance value and the difficulty in extraction of the effective mobility.

The AC characterisation (S-parameter and current gain) of a device with dimensions W=160 μm and L=20 μm was performed, and the values of gate and overlap capacitance extracted. The hybrid-pi model used was conceived for silicon MOSFETs and although simple to implement, is too simplistic for a TFT device. The obtained AC model had better agreement for frequencies lower than the f_T, and can be used as a rough estimation for a small signal analysis of the device. However, by not taking into account non-idealities like the contact resistance, extra poles and zeros created due to their connections were not described in the model. The variation in those connections affects the fitting in a significant way as the MOSFET model has an error of 0.12, 9.89, 24.8, and 18.3 for the S_{11}, S_{21}, S_{22} and h_{21} parameters respectively. The h_{21} parameter error depends mostly on the S_{22}, and S_{21} parameters, for this device, and the bad fitting of the S_{21} parameter (17.8 for the working frequencies) due to the extra poles and zeros is reflected on the bad fitting of the h_{21} parameter (15.6 for the working frequencies).

Future perspectives

A thorough physical characterisation and extraction of sub-gap density of states could be performed in the future, to analyse the electrical properties and obtain a better understanding of the device. This could lead to a more consistent model for the TFT, and possibly confirm some of the conjectures theorized on this project. For a better description of the high frequency behaviour, a small signal model that includes the contact resistance and other parasitics should be used. The optimisation of these models could also lead to its future application in circuit design.

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A

Appendix 1

A.0.1 S Parameter equations

A.0.1.1 S_{11}

$$S_{11} = \frac{b_1}{a_1} = \frac{z_{in} - z_0}{z_{in} + z_0} \tag{A.1}$$

Where $z_0 = 50\Omega$ is the characteristic impedance and $g_0 = \frac{1}{Z_0}$. As the value of z_0 is significantly smaller than r_o, we can assume that $z_0 // r_o \approx z_0$. The equation for S_{11} can then be rewritten as:

$$S_{11} \approx -\frac{-{g_0}^2 + C_{ch}\, g_0\, s + C_{ovd}\, g_m\, s + C_{ch}\, C_{ovd}\, s^2}{{g_0}^2 + C_{ovd}\, g_m\, s + (2\, C_{ovd} + C_{ch})\, g_0\, s + C_{ch}\, C_{ovd}\, s^2} \tag{A.2}$$

A.0.1.2 S_{12}

$$S_{12} = \frac{b_1}{a_2} = \frac{V_{in} - I_{in}.z_0}{V_o + I_o.z_0} = \frac{I_{in}(z_{in} - z_0)}{2V_o} \tag{A.3}$$

A.0.1.3 S_{21}

$$S_{21} = \frac{b_2}{a_1} = \frac{2V_o}{I_{in}(z_{in} + z_0)} \tag{A.4}$$

$$S_{21} = -\frac{2\, g_o\, (g_m - C_{ovd}\, s)}{{g_o}^2 + (C_{ch} + C_{ovs})\, g_o\, s + C_{ovd}\, g_m\, s + 2\, C_{ovd}\, g_o\, s + (C_{ch} + C_{ovs})\, C_{ovd}\, s^2} \tag{A.5}$$

A.0.1.4 S_{22}

$$S_{22} = \frac{b_2}{a_2} = \frac{V_o - I_o.z_0}{V_o + I_o.z_0} = \frac{z_{out} - z_0}{z_{out} + z_0} \tag{A.6}$$

$$S_{22} = \frac{go^2 + ((C_{ch} + C_{ovs})g_o - C_{ovd}g_m)s - C_{ovd}(C_{ch} + C_{ovs})s^2}{go^2 + ((C_{ch} + C_{ovs})g_o + C_{ovd}g_m + 2C_{ovd}g_o)s + C_{covd}(C_{ch} + C_{ovs})s^2} \tag{A.7}$$

A.0.2 Current gain

We are also able to obtain the h_{21} parameter (current gain) in terms of S-Parameters, resulting in the equation:

$$h_{21} = \frac{2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{A.8}$$

B

Appendix 2

B.1 Matlab scripts for Model

B.1.1 DC Model

B.1.1.1 Transfer curve fitting

```
1
2  %Load measured current/voltage values and extracted contact resistance/DeltaL values
3  load('')
4
5  syms IDS
6
7  % Constant values
8  VDS=0.1;
9  W=20E-6;
10 m=2
11 alpha=2.55
12 K=4.5E-8;
13
14 % Transistor change (channel length and threshold voltage)
15 for z=1:3
16 eles=[40E-6;80E-6;160E-6];
17 vts=[5.5;6;6];
18 Vt=vts(z);
19
20 % Gate bias change (0-18 V)
21 for j=0:18
22 VGS=j;
23 a=j+1;
24 vgs(a)=j;
25
26 %For low VGS (subthreshold or near VT)
27 if VGS-Vt<1
28 %Value assumed to be similar to lowest VGS-Vt applied
29 RDS=2.8/(20E-6);
30 L=eles(z);
31 end
32
33 % For high VGS (1 V above VT)
34 if VGS-Vt>=1
35 % Contact resistance and DeltaL values
36 RdsW=['']
37 Lvar=['']
38 Y = round( Vt , 0 );
39 G=j-(Y);
40 RDS=RdsW(G)/W;
41 L=eles(z)+Lvar(G);
42 end
43
```

```
%Model equation (here VDSint does not affect the fitting)
VDSint=(VDS^(-m)+(VGS-Vt)^(-m))^(-1/m);
eqn=-IDS+K*(W/L)*((VGS-(IDS*RDS/2)-Vt)^(alpha-1))*(VDSint-(IDS*RDS))==0;
sol = vpasolve(eqn,IDS);

%Model is above-threshold for VGS>Vt
if j-Vt<0
current(a)=0;
else
current(a)=sol;
end
end

%Plot Model
plot(vgs,current,'color','k');hold on;
%Plot Data
plot(' ');hold on;
end
```

B.1.1.2 Output curve fitting

```
load('correntenova.mat')
load('outputnova.mat')
load('alphak.mat')
syms IDS

% Constant Values
W=20E-6;
m=2.5;
alpha=2.55
K=4.5E-8;
Vt=6;
gammasat=1.87;
VA=450;
lambda=8.89E-8;
m=2.5;

% Gate bias change
for z=1:5
vgs=[6.01;7;8;9;10];
VGS=vgs(z);
x=vgs(z)-Vt;
Y = round( x , 0 );
% Variable contact resistance and length variation
RdsW=[' '];
Lss=[' '];
RDS=RdsW(Y+2)/(20E-6);
L=eles+Lss(8-z);

% Drain bias change
for j=0:72
a=(j)+1;
```

```
VDS=output_80(a,1);
vds(a)=output_80(a,1);


%LINEAR
VDSint=(VDS^(-m)+(VGS-Vt)^(-m))^(-1/m);
eqn=-IDS+K*(W/L)*((VGS-(IDS*RDS/2)-Vt)^(alpha-1))*(VDSint-(IDS*RDS))-((1-1/alpha)*(
    VDSint-IDS*RDS)^alpha)==0;
sola = vpasolve(eqn,IDS);
solad(a)=sola;
if vgs(z)-Vt>=VDS
finalplot(a)=double(sola);
end

%SATURATION
xcm=1+(lambda*VDS/L);
eqn = -IDS+((K/alpha)*gammasat*(W/L)*xcm)*((x-(RDS/2)*IDS)^alpha)==0;
solx = vpasolve(eqn, IDS,1E-9);
solve(a)=solx;
if vgs(z)-Vt<VDS
finalplot(a)=double(solx);
end
end

%Plot Model
plot(output_80(:,1),output_80(:,9),'.','color','b');hold on;
plot(vds,finalplot,'k');hold on;
plot(' ','.','color','b');hold on;
xlabel('VDS (V)') % x-axis label
ylabel('IDS (A)') % y-axis label
legend('Data','Model')
end
```

B.1.2 AC Model

B.1.2.1 S_{11}

```
syms go_ gm_ scovd scch
load('S11_160.mat')
%Values
S11=-(-go_^2+scch*go_+scovd*gm_+scch*scovd)/(go_^2+scovd*gm_+(2*scovd+scch)*go_+scch
    *scovd)
x=1E3:1000:2E9;
go=1/50;
gm=4E-6;
covd=3E-13;
cch=1.3E-12;
s=2*pi*i*x;
%Magnitude
s11=-(-go^2+s.*cch*go+s.*covd*gm+cch*covd.*s.^2)./(go^2+covd*gm.*s+(2*covd+cch)*go.*
    s+cch*covd.*s.^2);
H11 = tf([-cch*covd,-covd*gm+cch*go,go^2],[cch*covd,(2*covd+cch)*go+covd*gm,go^2]);
```

```
[mag,phase,wout]=bode(H11,{10E3,10E9});
freq=wout./(2*pi);
semilogx(freq,20*log10(squeeze(mag)),'k');hold on;
semilogx(S11_Frequency_160(:,1),S11_Frequency_160(:,2),'.');
axis([1E3 5E9 -0.7 1])
title('Magnitude of S11 Parameter')
xlabel('Frequency (Hz)') % x-axis label
ylabel('Magnitude (dB)') % y-axis label
legend('Model','Data')
hold off;

MagnitudeS11model=20*log10(squeeze(mag));
MagnitudeS11data=S11_Frequency_160(:,2);

%Phase
BODE11=bodeplot(H11,{10E3,10E9},'k');hold on;
setoptions(BODE11,'FreqUnits','Hz','MagVisible','off','PhaseMatching', 'on', '
    PhaseMatchingValue', 0);
semilogx(S11_Frequency_160(:,1),S11_Frequency_160(:,3),'.');hold on;
axis([1E3 5E9 -25 10])
legend('Model','Data')
hold off;
```

B.1.2.2 S_{21}

```

%Values
load('S21_160.mat')
s=2*pi*i*S21_Frequency_160(:,1);
go=1/50;
gm=4E-6;
cch=1.3E-12;
covd=3E-13;
%Magnitude
s21=-(2*go*(gm-covd.*s))./(go^2+cch*go.*s+covd*gm.*s+2*covd*go.*s+covd*cch.*s.^2);
s21_=mag2db(abs(s21));
semilogx(S21_Frequency_160(:,1),s21_,'k');hold on;
semilogx(S21_Frequency_160(:,1),S21_Magnitude_160,'.');hold on;
title('Magnitude of S21 Parameter')
xlabel('Frequency (Hz)') % x-axis label
ylabel('Magnitude (dB)') % y-axis label
legend('Model','Data')
hold off;
gm=db2mag(-68)/100

%Phase
H21 = tf([2*go*covd,-2*go*gm],[cch*covd,(2*covd+cch)*go+covd*gm,go^2]);
BODE21=bodeplot(H21,{10E3,10E9},'k');hold on;
setoptions(BODE21,'FreqUnits','Hz','MagVisible','off','PhaseMatching', 'on', '
    PhaseMatchingValue', 0);
semilogx(S21_Frequency_160(:,1),S21_Phase_160(:,1),'.')
legend('Model','Data')
```

```
%semilogx(x,phase(s11),'y')
%axis([1E3 5E9])
hold off;
```

B.1.2.3 S_{22}

```
%Values
syms go gm scovd scch S22 s covd cch
load('S22_160.mat')
S22=simplify(((1/(gm*(s*covd/(s*cch+s*covd+go))+s*covd-s*covd*(s*covd/(s*cch+s*covd+
    go))))-(1/go))/((1/(gm*(s*covd/(s*cch+s*covd+go))+s*covd-s*covd*(s*covd/(s*cch+s
    *covd+go))))+(1/go)),'Steps',10)
s=2*pi*i*S22_Frequency_160(:,1);
go=1/50;
gm=0.000004;
cch=1.3E-12;
covd=3E-13;
%Magnitude
s22=((1./(gm.*(s.*covd./(s.*cch+s.*covd+go))+s.*covd-s.*covd.*(s.*covd./(s.*cch+s.*
    covd+go))))-(1/go))./((1./(gm.*(s.*covd./(s.*cch+s.*covd+go))+s.*covd-s.*covd.*(
    s.*covd./(s.*cch+s.*covd+go))))+(1/go));
s22_=mag2db(abs(s22));
semilogx(S22_Frequency_160(:,1),s22_,'k');hold on;
semilogx(S22_Frequency_160(:,1),S22_Frequency_160(:,2),'.');hold on;

title('Magnitude of S22 Parameter')
xlabel('Frequency (Hz)') % x-axis label
ylabel('Magnitude (dB)') % y-axis label
legend('Model','Data')
axis([1E3 1E9 -0.04 0.04]); hold off;

%Phase
H22 = tf([cch*covd,go*cch-covd*gm,go^2],[cch*covd,(2*covd+cch)*go+covd*gm,go^2]);
BODE22=bodeplot(H22,{10E3,10E9},'k');hold on;
setoptions(BODE22,'FreqUnits','Hz','MagVisible','off','PhaseMatching', 'on', '
    PhaseMatchingValue', 0, 'YLimMode','manual','Ylim',[-100,100]);
semilogx(S22_Frequency_160(:,1),(S22_Phase_160(:,1)-S22_Phase_160OPEN(:,1)),'.')
legend('Model','Data')
%semilogx(x,phase(s11),'y')
%axis([1E3 5E9])
hold off;
```

B.1.2.4 h_{21}

```
cd('FILES')
load('S11_160.mat')
load('S12_160.mat')
load('S21_160.mat')
load('S22_160.mat')
s=2*pi*i*S21_Frequency_160(:,1);
```

```
go=1/50;
gm=0.000004;
cch=1.2E-12;
covd=3E-13;


[x,y] = pol2cart(deg2rad(wrapTo360(Fase(:,1))),db2mag(Magnitude(:,1)));
z11= x+y*i;
[x,y] = pol2cart(deg2rad(wrapTo360(S12_Phase_160(:,1))),db2mag(S12_Magnitude_160
    (:,1)));
z12= x+y*i;
[x,y] = pol2cart(deg2rad(wrapTo360(S22_Frequency_160(:,3))),db2mag(S22_Frequency_160
    (:,2)));
z22= x+y*i;
[x,y] = pol2cart(deg2rad(wrapTo360(S21_Phase_160(:,1))),db2mag(S21_Magnitude_160
    (:,1)));
z21= x+y*i;


H21complex=mag2db(abs((-2.*z21)./((1-z11).*(1+z22)+z12.*z21)));


H21=(-2.*S21_Magnitude_160(:,1))./(((1-S11_Frequency_160(:,2)).*(1+S22_Frequency_160
    (:,2))+S12_Magnitude_160(:,1).*S21_Magnitude_160(:,1)));
semilogx(S21_Frequency_160(:,1),H21complex);hold off;


h21=(s.*covd-gm)./(s.*(covd+cch));
h21_=(mag2db(abs(h21)));

%Plot graph
semilogx(S21_Frequency_160(:,1),H21complex,'.');hold on;
semilogx(S21_Frequency_160(:,1),h21_,'k');
title('Modeling of H21 Parameter')
xlabel('Frequency (Hz)') % x-axis label
ylabel('Magnitude (dB)') % y-axis label
legend('Data','Model')
hold off;
```

C

Appendix 3

C.1 Optical microscope images

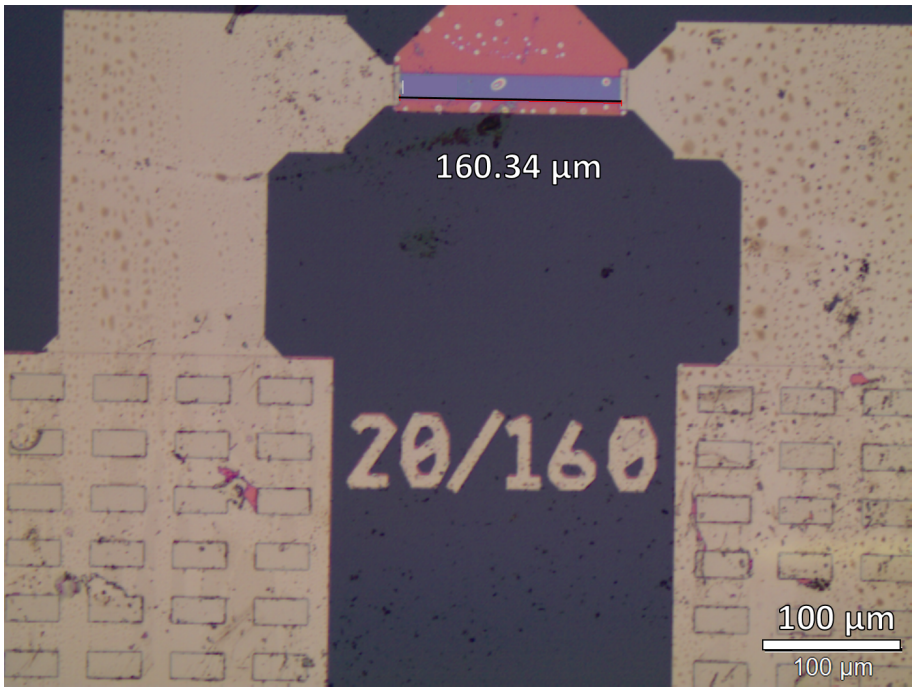

Figure C.1: Image extracted from the optic microscope, with a scale of 100µm, of the thin film transistor channel with dimensions W=20 μm and L=160 μm

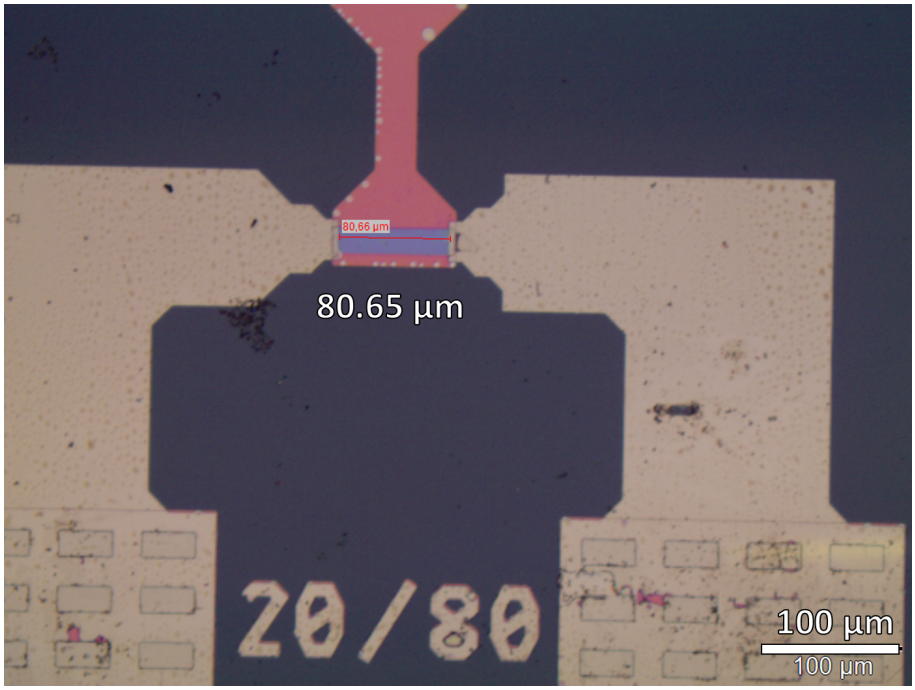

Figure C.2: Image extracted from the optic microscope, with a scale of 100µm, of the thin film transistor channel with dimensions W=20 μm and L=80 μm

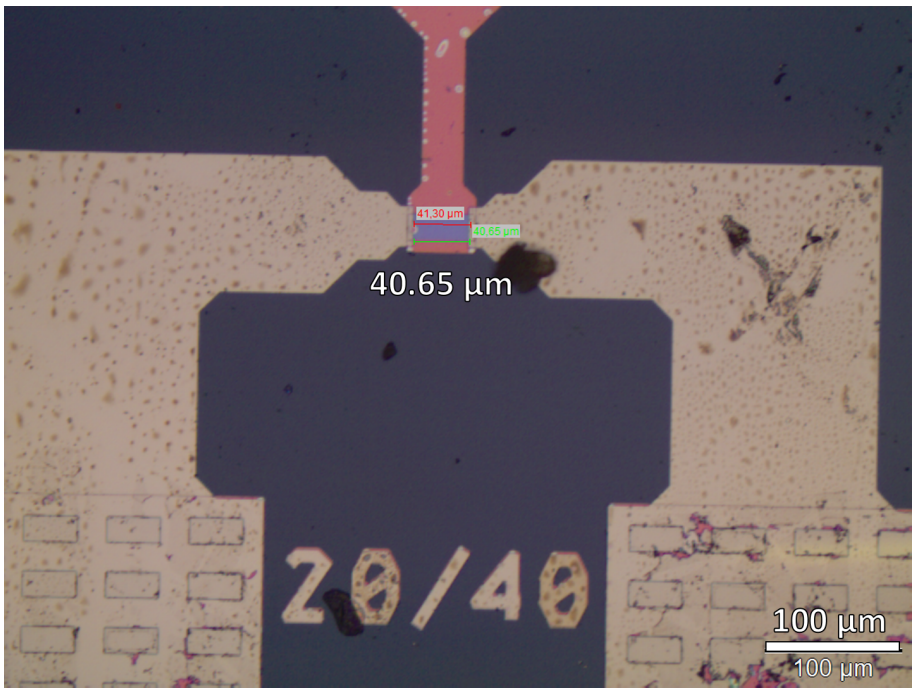

Figure C.3: Image extracted from the optic microscope, with a scale of 100µm, of the thin film transistor channel with dimensions W=20 μm and L=40 μm

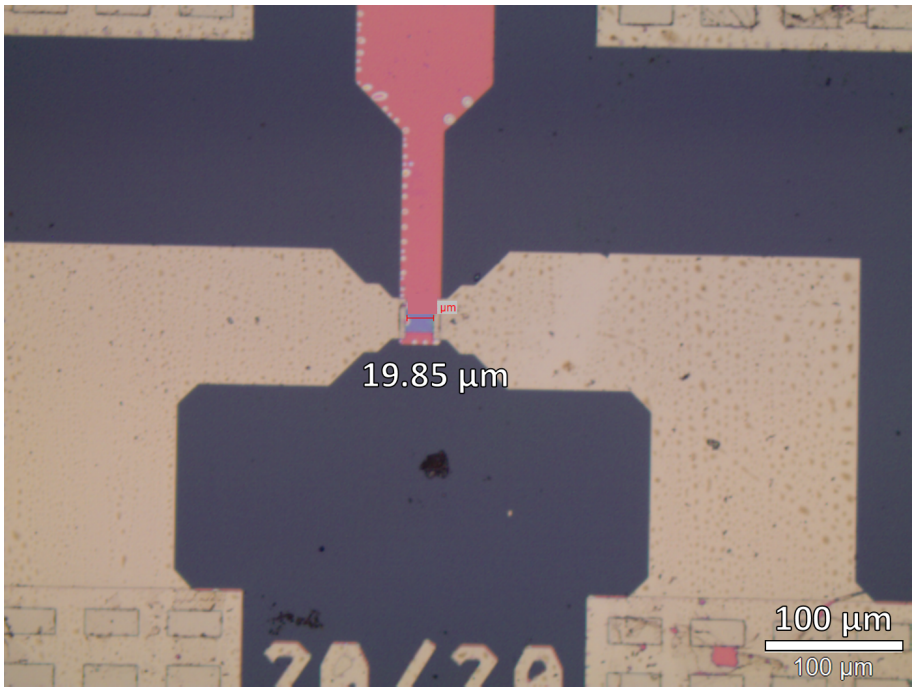

Figure C.4: Image extracted from the optic microscope, with a scale of 100µm, of the thin film transistor channel with dimensions W=20 μm and L=20 μm

I

Annex 1